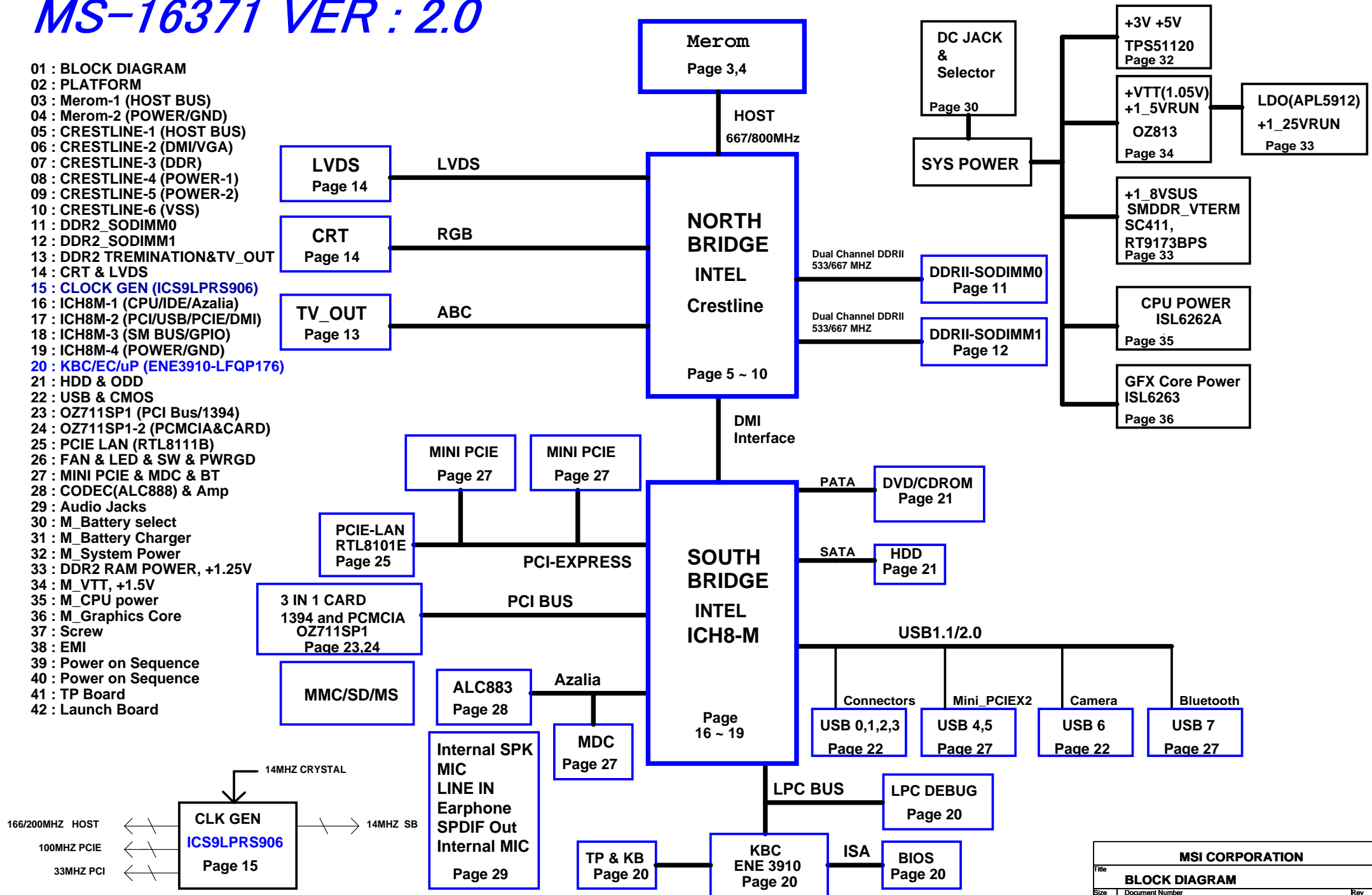


# MS-16371 VER: 2.0

- 01 : BLOCK DIAGRAM
- 02 : PLATFORM
- 03 : Merom-1 (HOST BUS)
- 04 : Merom-2 (POWER/GND)
- 05 : CRESTLINE-1 (HOST BUS)
- 06 : CRESTLINE-2 (DMI/VGA)
- 07 : CRESTLINE-3 (DDR)
- 08 : CRESTLINE-4 (POWER-1)
- 09 : CRESTLINE-5 (POWER-2)
- 10 : CRESTLINE-6 (VSS)
- 11 : DDR2\_SODIMM0
- 12 : DDR2\_SODIMM1
- 13 : DDR2 TREMINATION&TV\_OUT
- 14 : CRT & LVDS
- 15 : CLOCK GEN (ICS9LPRS906)
- 16 : ICH8M-1 (CPU/IDE/Azalia)
- 17 : ICH8M-2 (PCI/USB/PCIE/DMI)
- 18 : ICH8M-3 (SM BUS/GPIO)
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- 20 : KBC/EC/uP (ENE3910-LFQP176)
- 21 : HDD & ODD
- 22 : USB & CMOS
- 23 : OZ711SP1 (PCI Bus/1394)
- 24 : OZ711SP1-2 (PCMCIA&CARD)
- 25 : PCIE LAN (RTL8111B)
- 26 : FAN & LED & SW & PWRGD
- 27 : MINI PCIE & MDC & BT
- 28 : CODEC(ALC888) & Amp
- 29 : Audio Jacks
- 30 : M\_Battery select
- 31 : M\_Battery Charger
- 32 : M\_System Power
- 33 : DDR2 RAM POWER, +1.25V
- 34 : M\_VTT, +1.5V
- 35 : M\_CPU power
- 36 : M\_Graphics Core
- 37 : Screw
- 38 : EMI
- 39 : Power on Sequence
- 40 : Power on Sequence
- 41 : TP Board
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Title	BLOCK DIAGRAM		
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## Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
VHORE	Core Voltage for Processor	VR_ON
+VTT	1.05 rail for Processor & 965GM I/O	PM_SLP_S3# ( RUN_ON )
+1_5VRUN	1.5V switched power rail(off in S3-S5)	PM_SLP_S3# ( RUN_ON )
+1_25VRUN	1.25V powe rail NB PLL and PXE (off in S3-S5)	+1_5VRUN
+3VRUN	3.3V switched power rail(off in S3-S5)	RUND ( RUN_ON )
+5VRUN	5.0V switched power rail(off in S3-S5)	RUND (RUN_ON )
SMDDR_VTERM	0.9V DDR Termination voltage (off in S4-S5)	PM_SLP_S3# ( RUN_ON )
+1_8VDIMM	1.8V power rail DDR (off in S4-S5)	PM_SLP_S4# ( DIMM_ON )
+3VSUS	3.3V power rail (off in S4-S5)	SUS_ON
+5VSUS	5.0V power rail (off in S4-S5)	SUS_ON
+3VALW	3.3V always on power rail	PWR_SRC
+5VALW	5.0V always on power rail	PWR_SRC
+V5_AUDIO	5.0V Power rail Audio codec(off in S3-S5)	RUND
VTT_G	Core Voltage for GMCH GPU	GFX_VR_EN

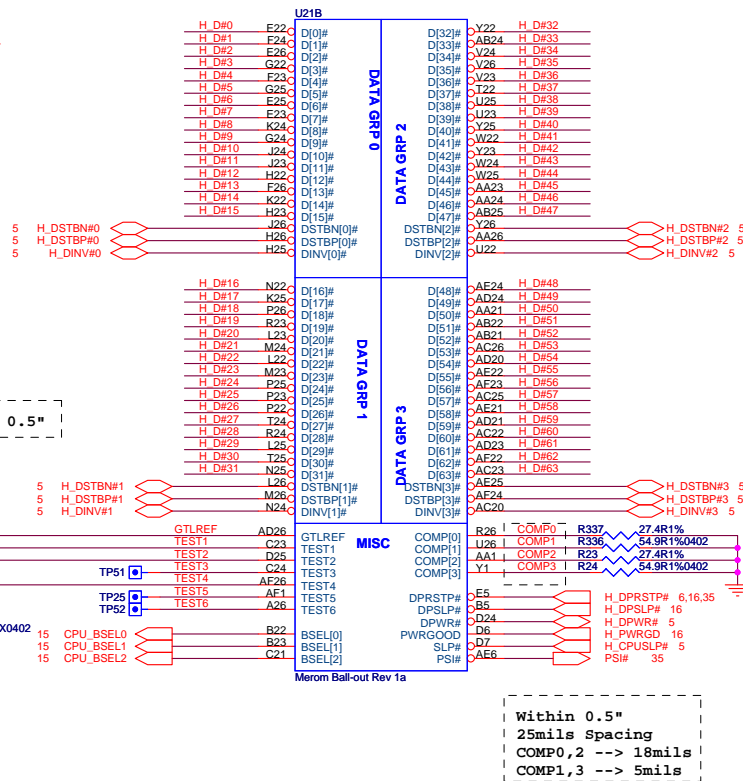
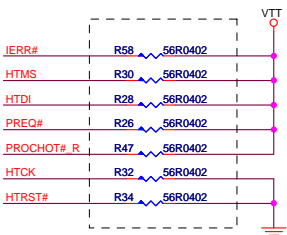
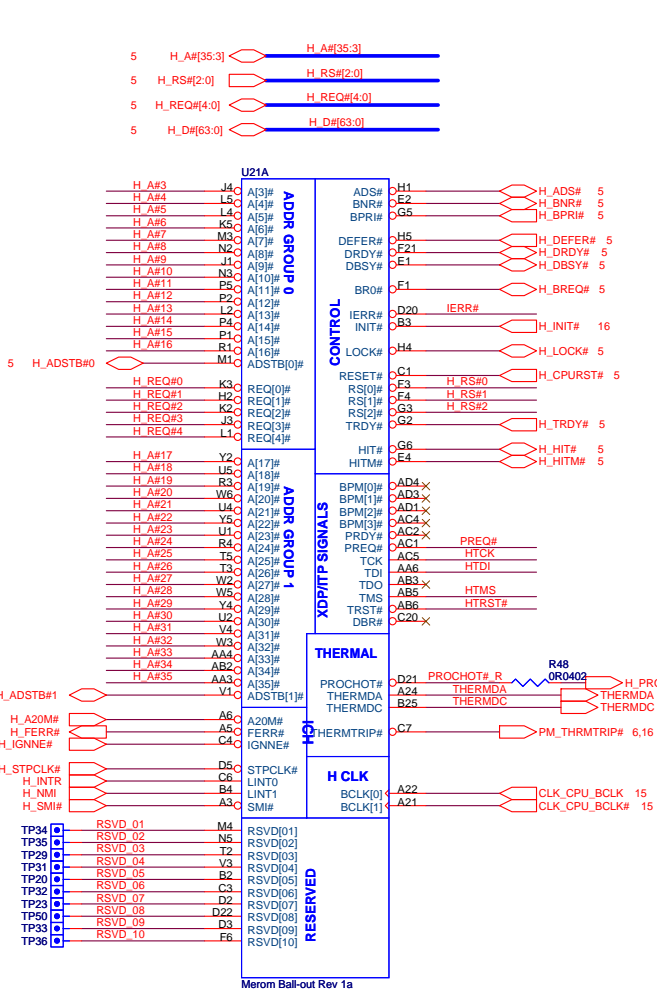
System Power consumption	
CPU Vcore	40W
3V	15W
5V	25W
Graphics Vcore	10W
1.5V	7W
1.05V	10W
PWR_SRC	107W(12A)

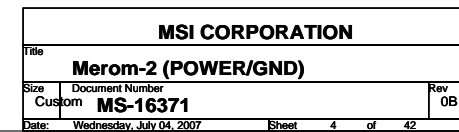
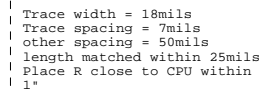
## POWER STATES

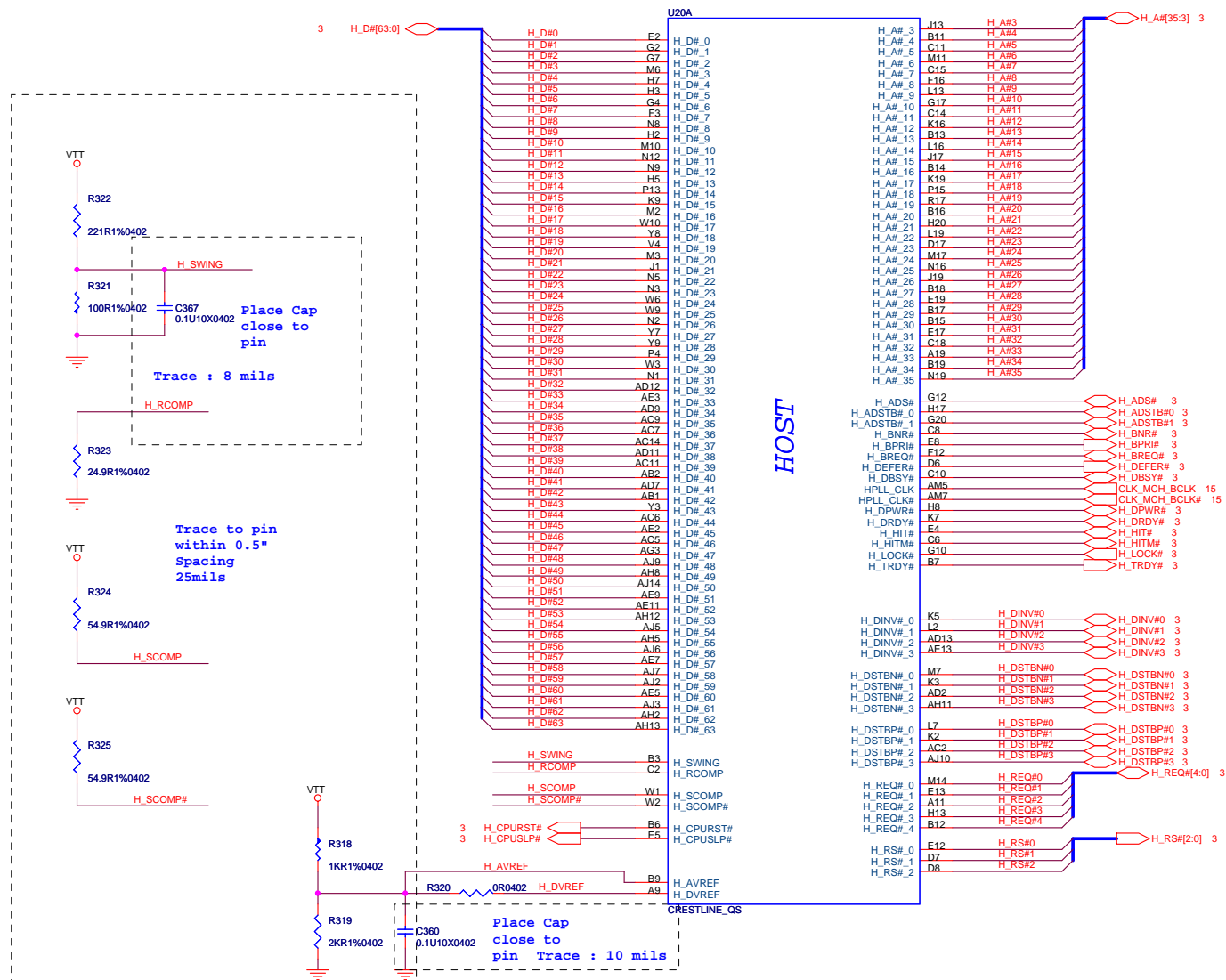
STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALWAYS	+V*SUS	+V*RUN	Clocks
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3( Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4( Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 / Soft OFF	LOW	LOW	LOW	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on then +V\*SUS will always keep high

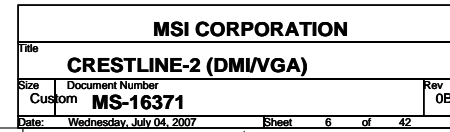
MSI CORPORATION		
Title		
PLATFORM		
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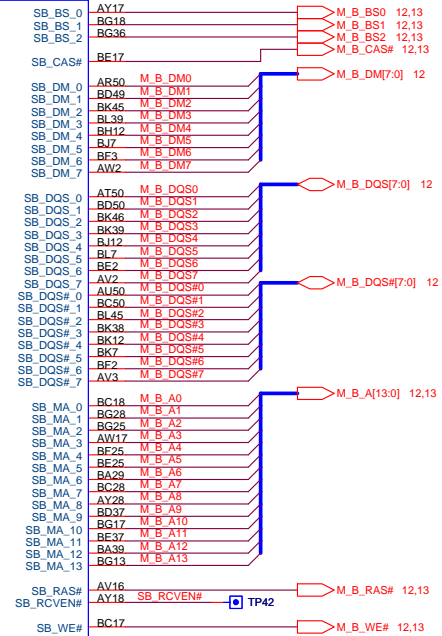
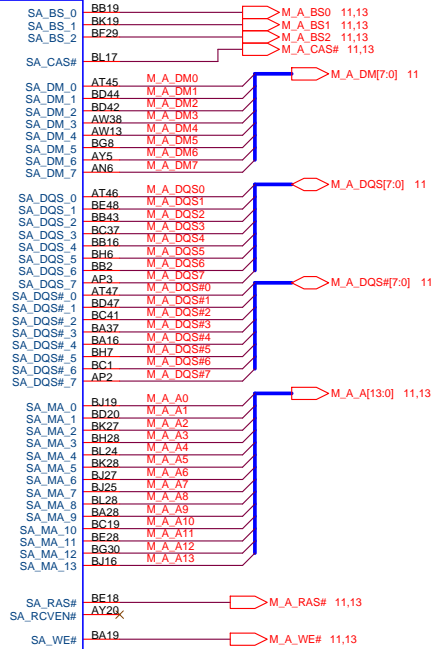


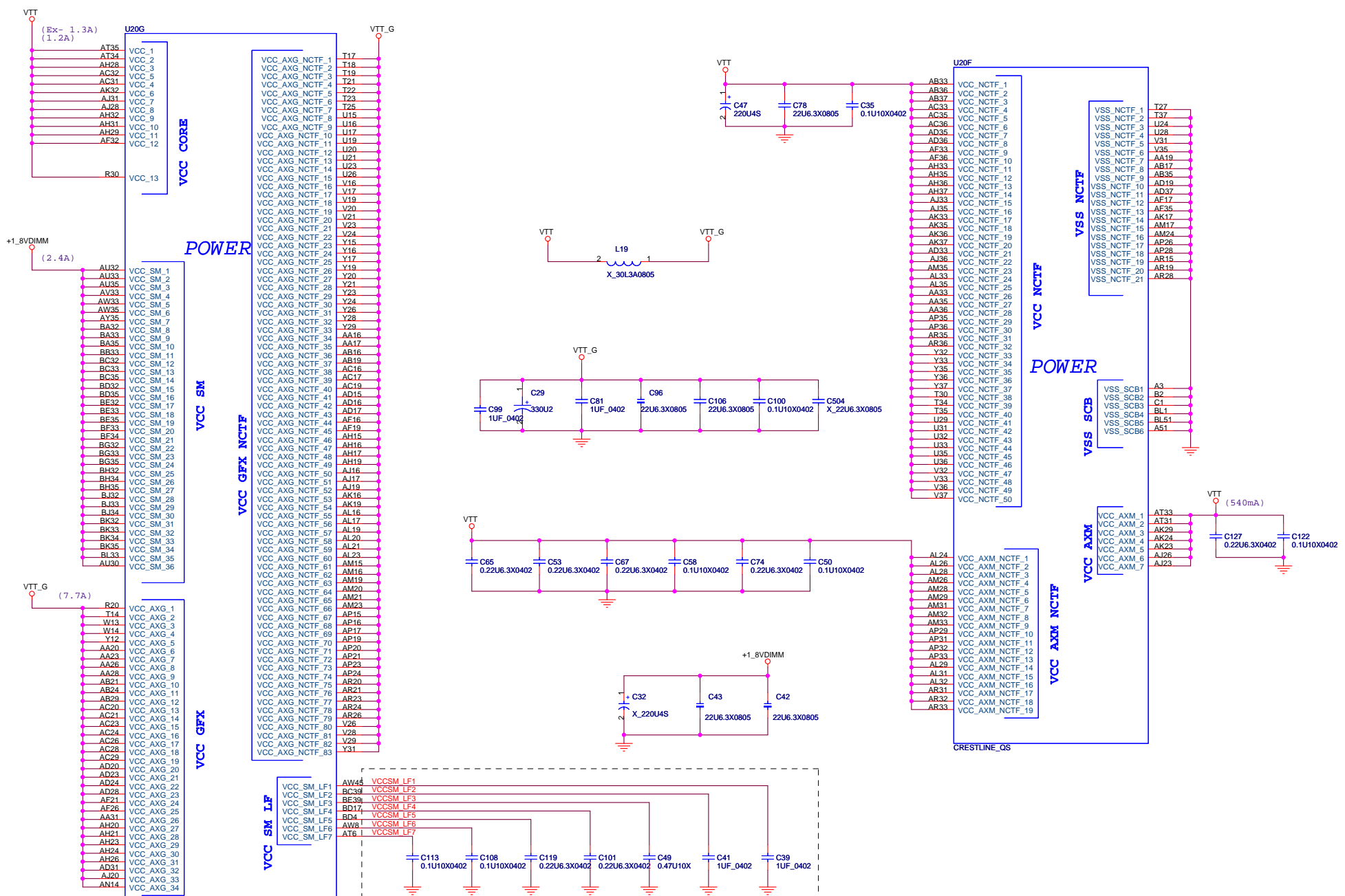




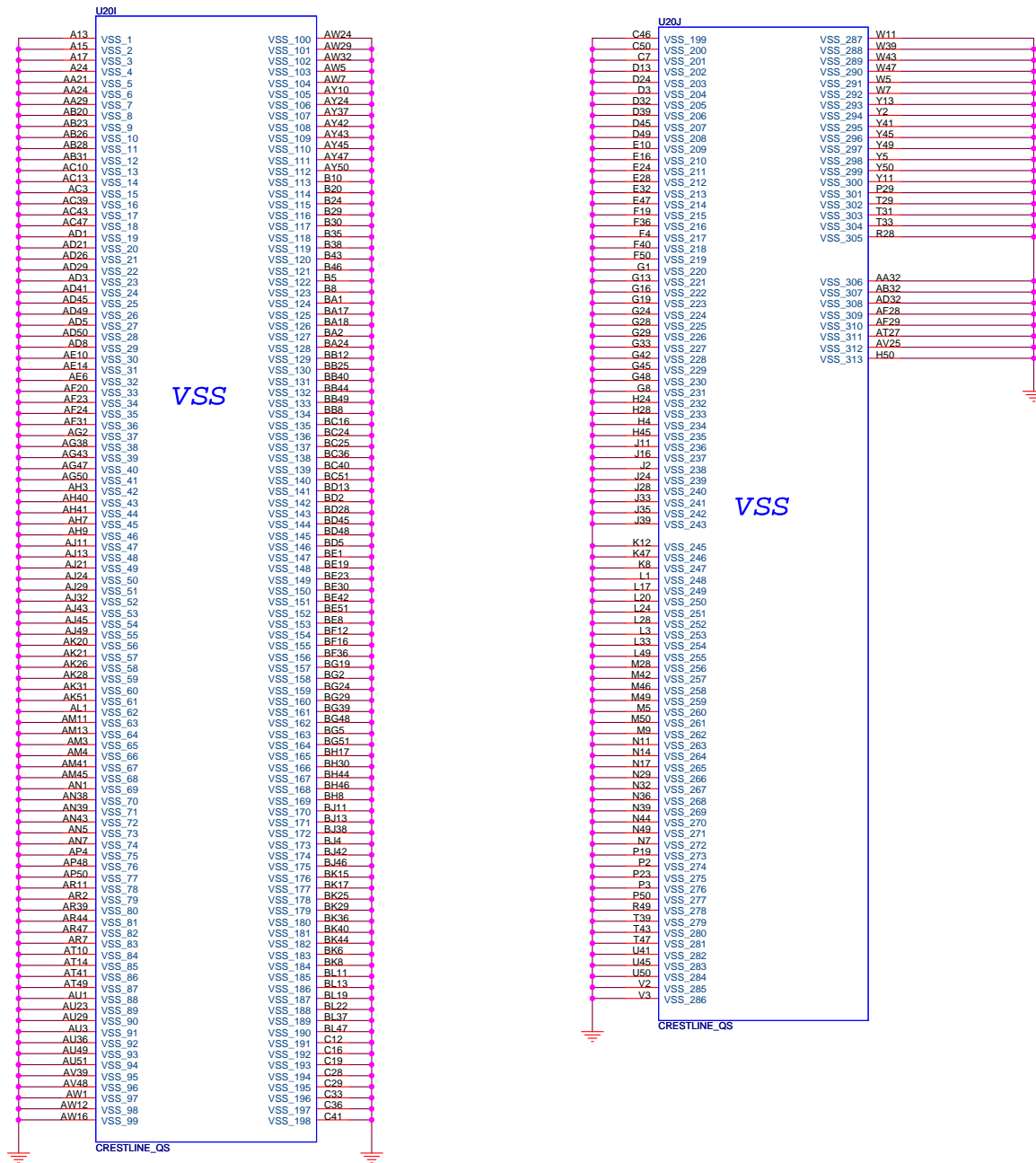
MSI CORPORATION			
Title	CRESTLINE-1 (HOST BUS)		
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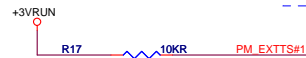
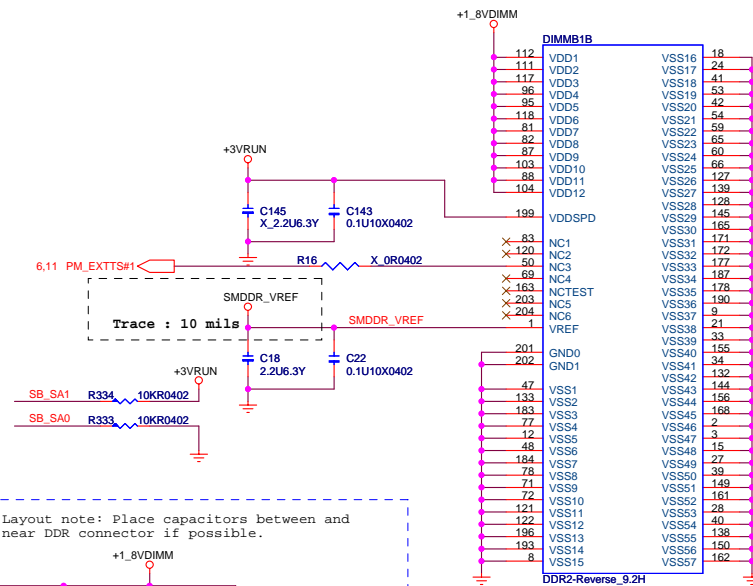
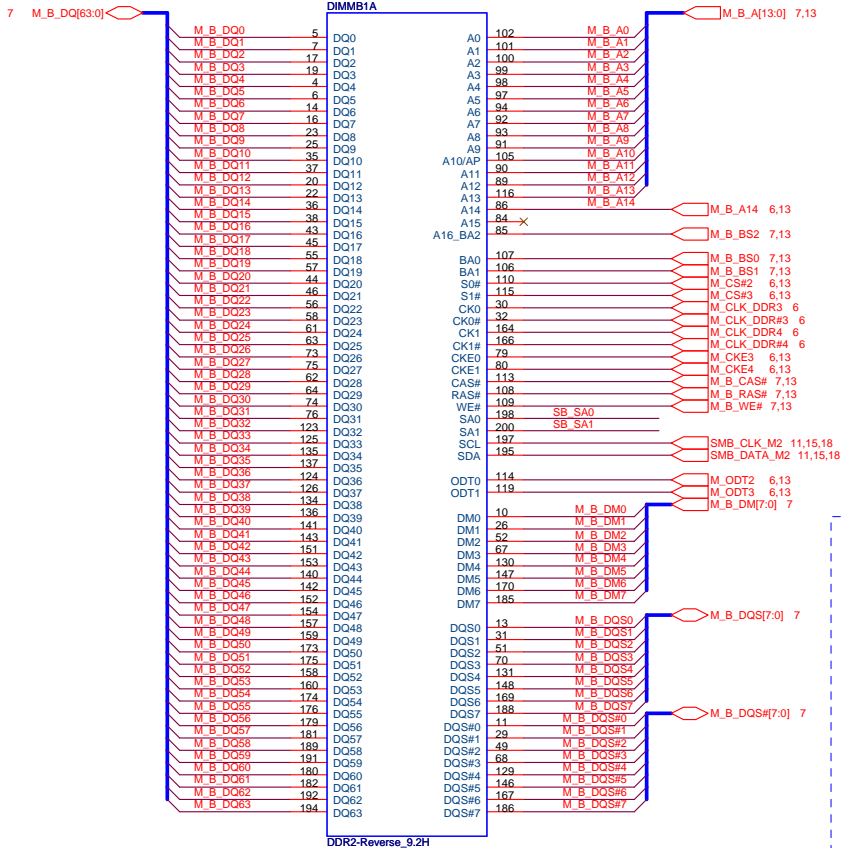


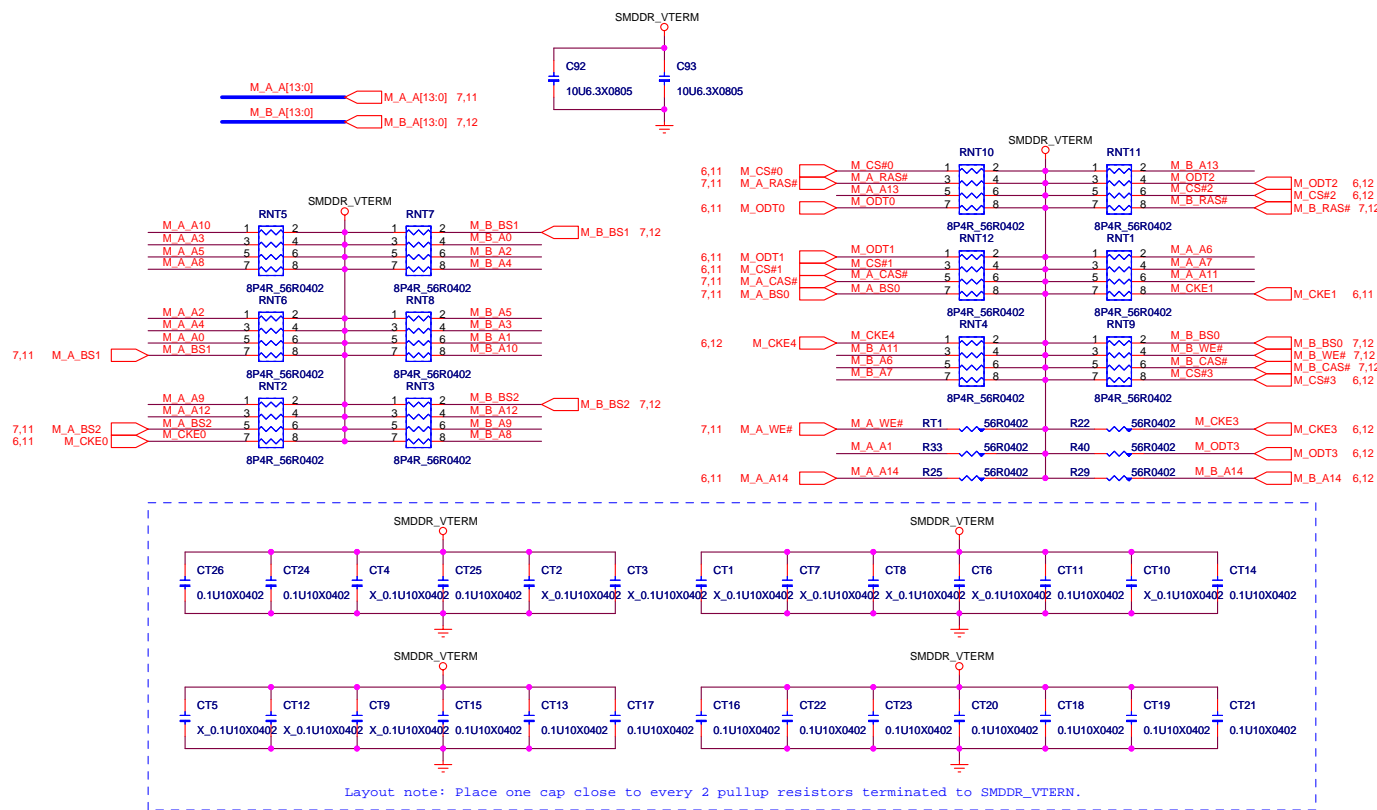




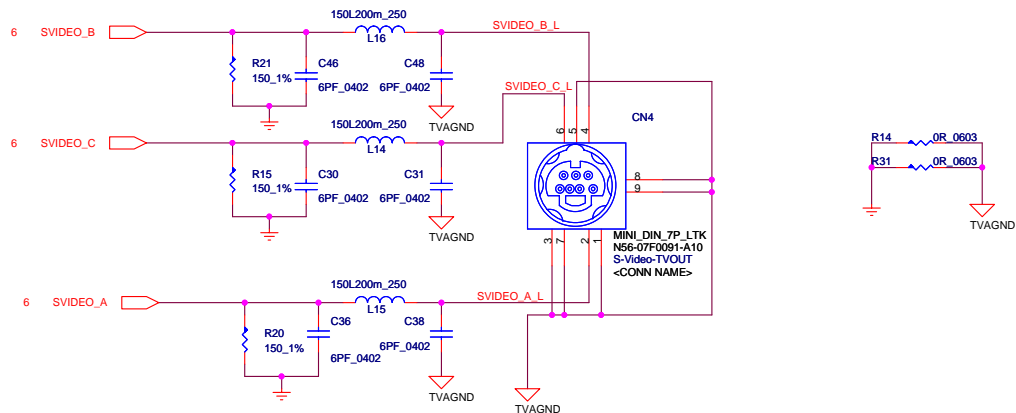






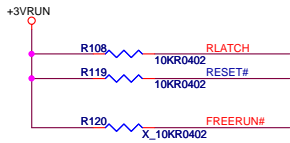


Video Filter SPEC:  
 $C = 6\text{pF} \pm 20\%$ ,  $16\text{V}$ ,  $0.603$   
 $L = 150\text{ohm}$  @  $100\text{MHz}$ ,  $100\text{mA}$  (min)



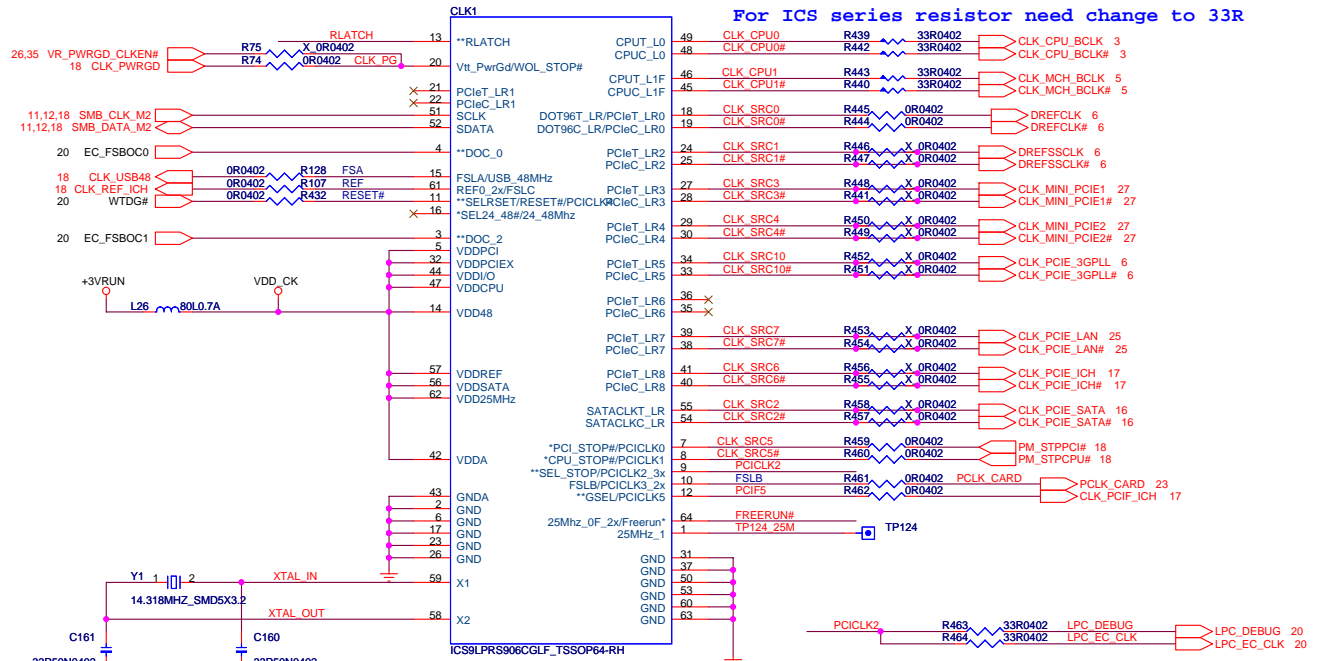
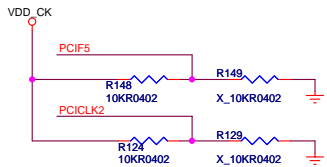
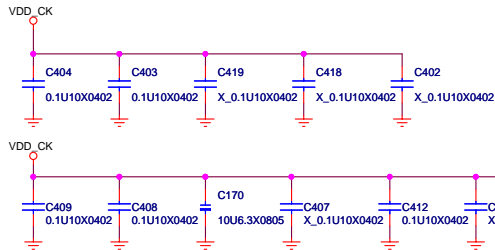
MSI CORPORATION			
Title	DDR2 TREMINATION&TV_OUT		
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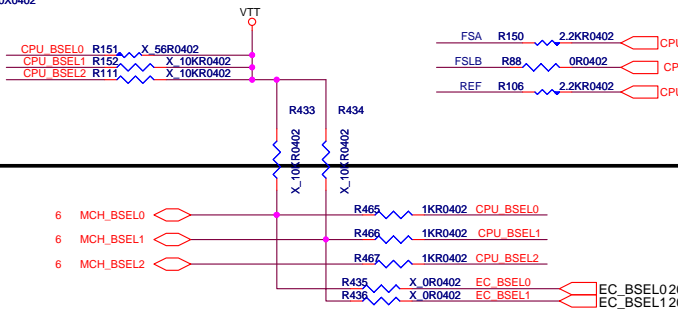


Strapping Configuration(SLG)

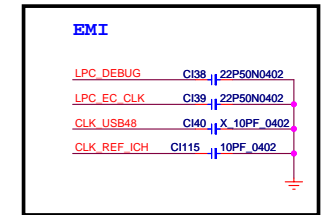
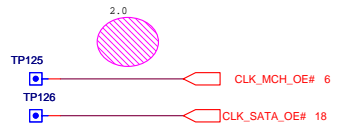
PIN#	High	Low
9	PIN7/8 PCI/CPU STOP	PIN7/8 PCICLK OUTPUT
11	PIN11 RESET#	PIN11 PCICLK
12	PIN18/19 DOT96MHz	PIN18/19 PCIE CLK0



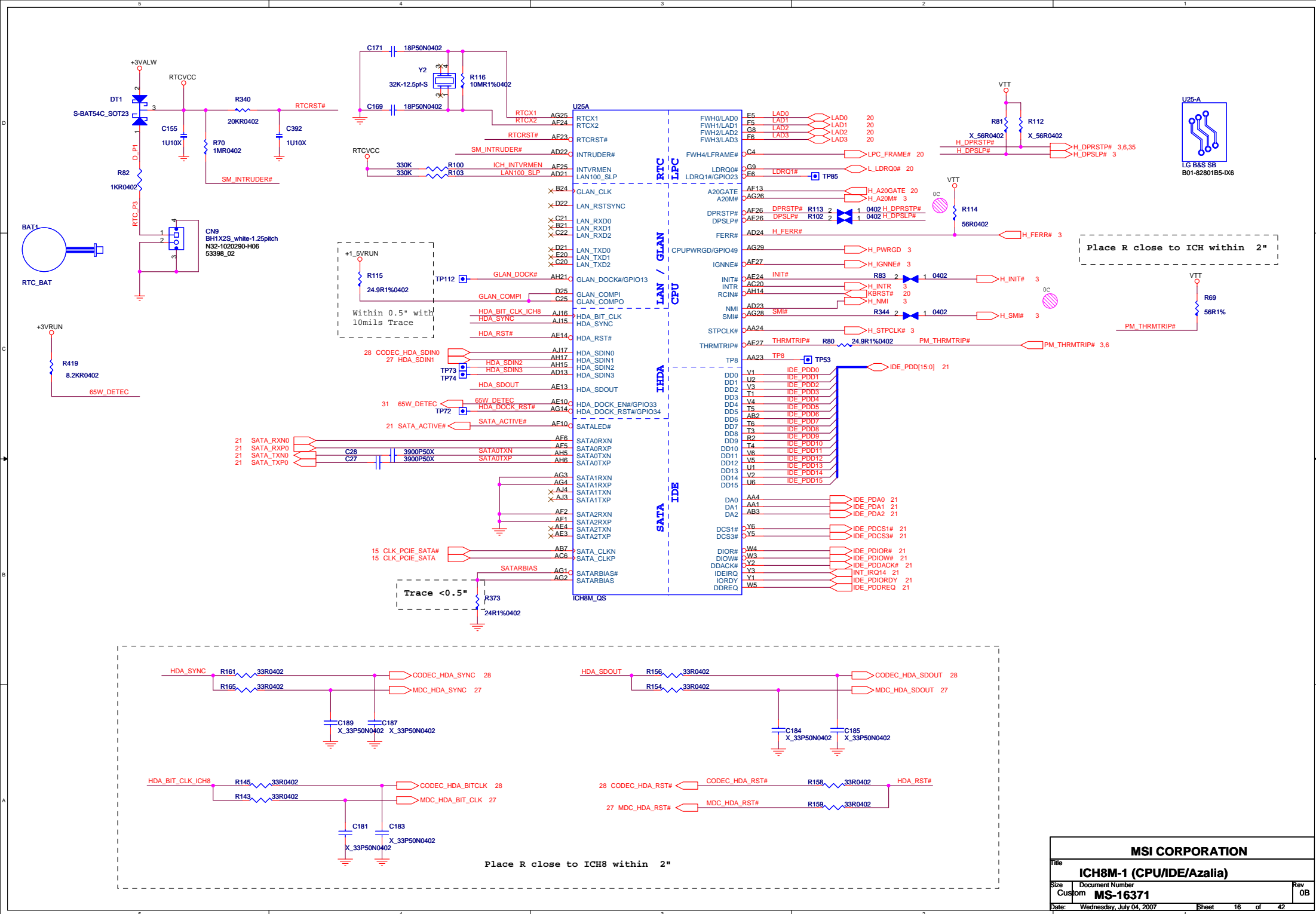
place within 500 mils  
of clock IC



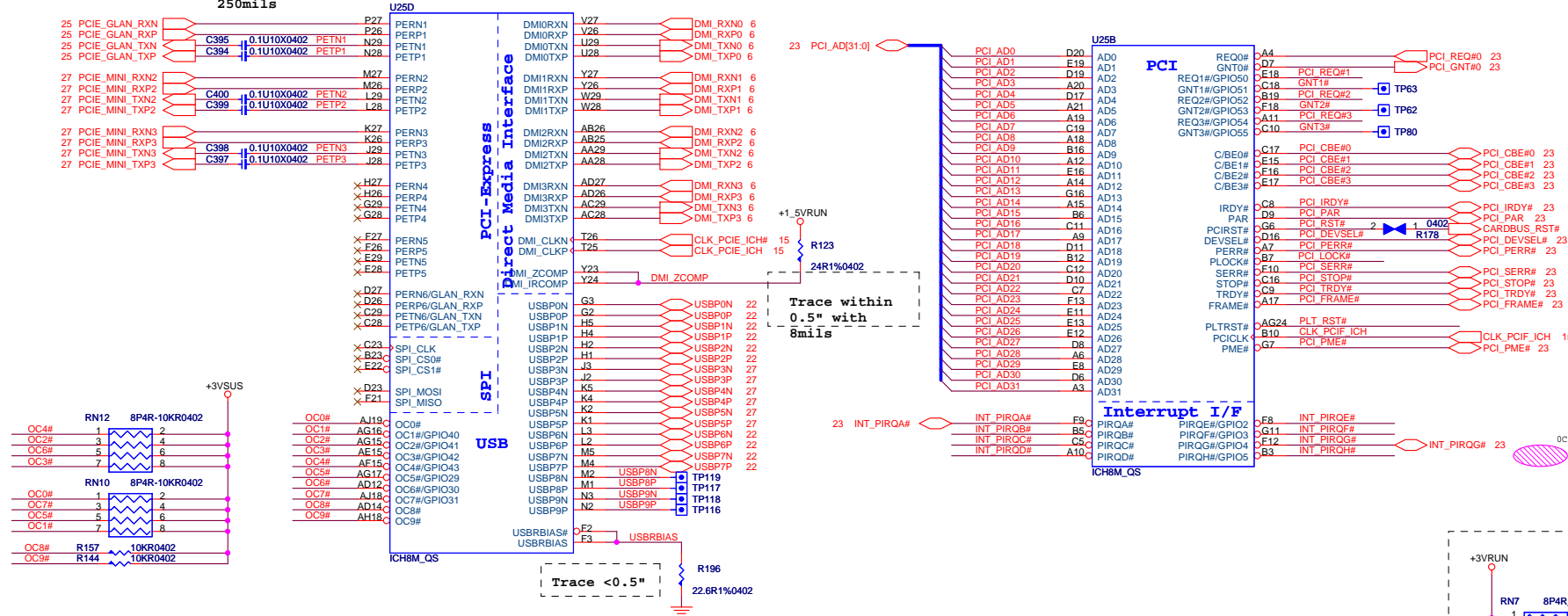
CPU Table			FSB Freq (MHz)
BSEL[2]	BSEL[1]	BSEL[0]	
L	H	H	667 MHz
L	H	L	800 MHz



MSI CORPORATION			
CLOCK Generator (CK505)			
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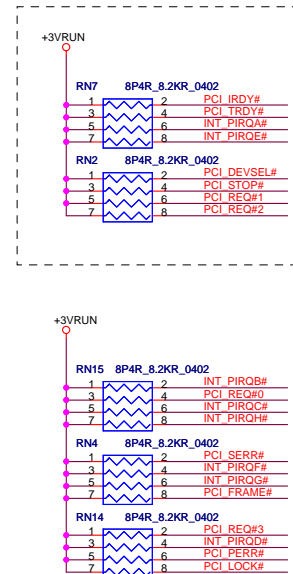
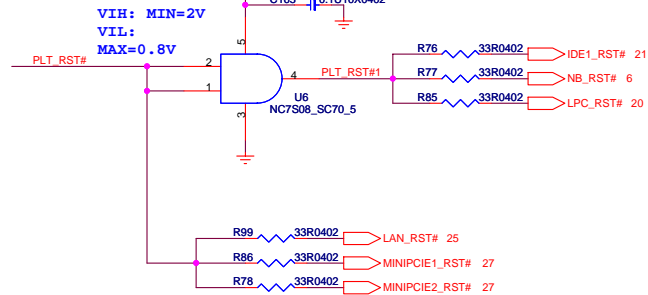


place Cap  
close to  
ICH8 within  
250mils



Trace within  
0.5" with  
8mils

Trace <0.5"



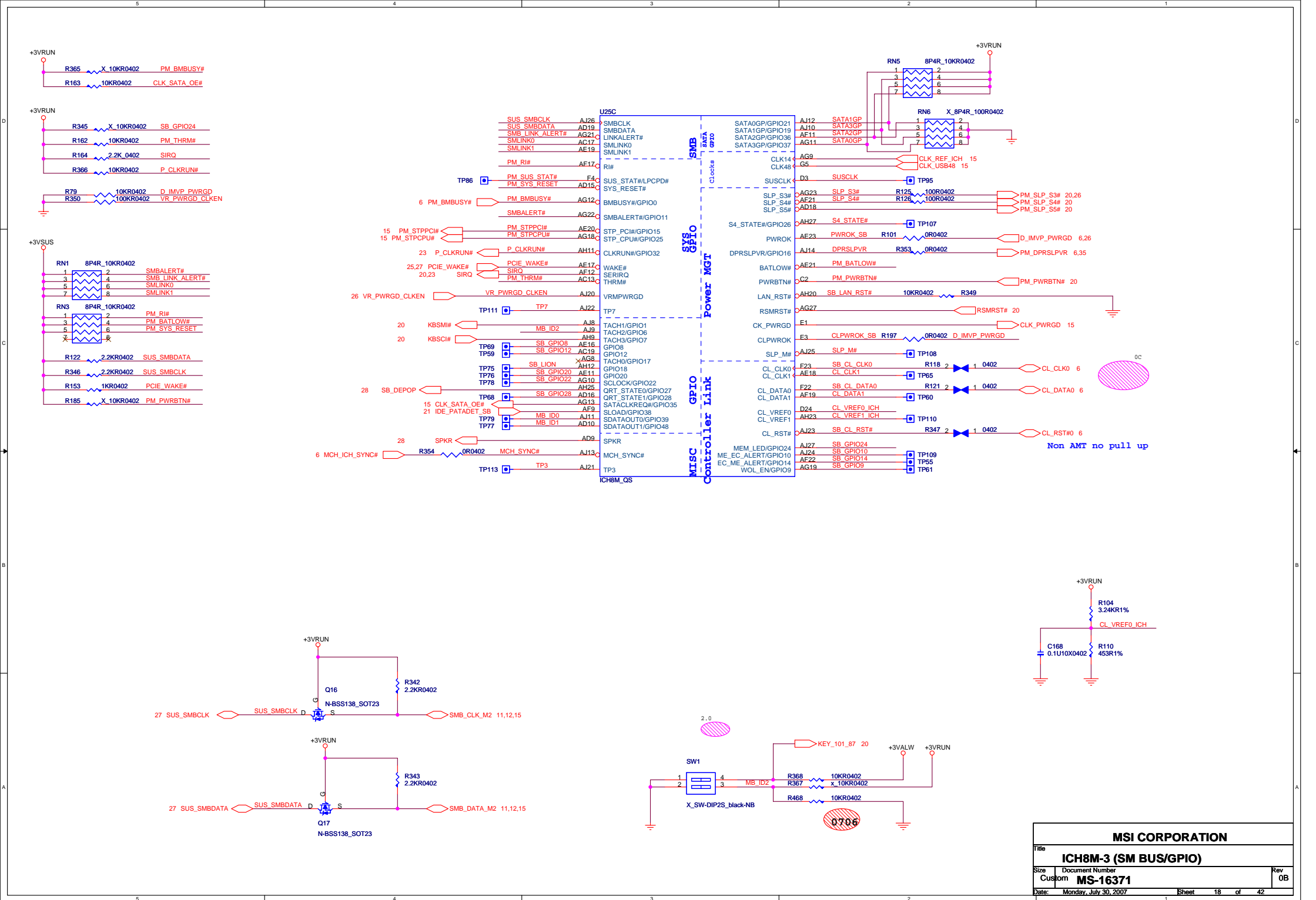
#### Strapping Configuration

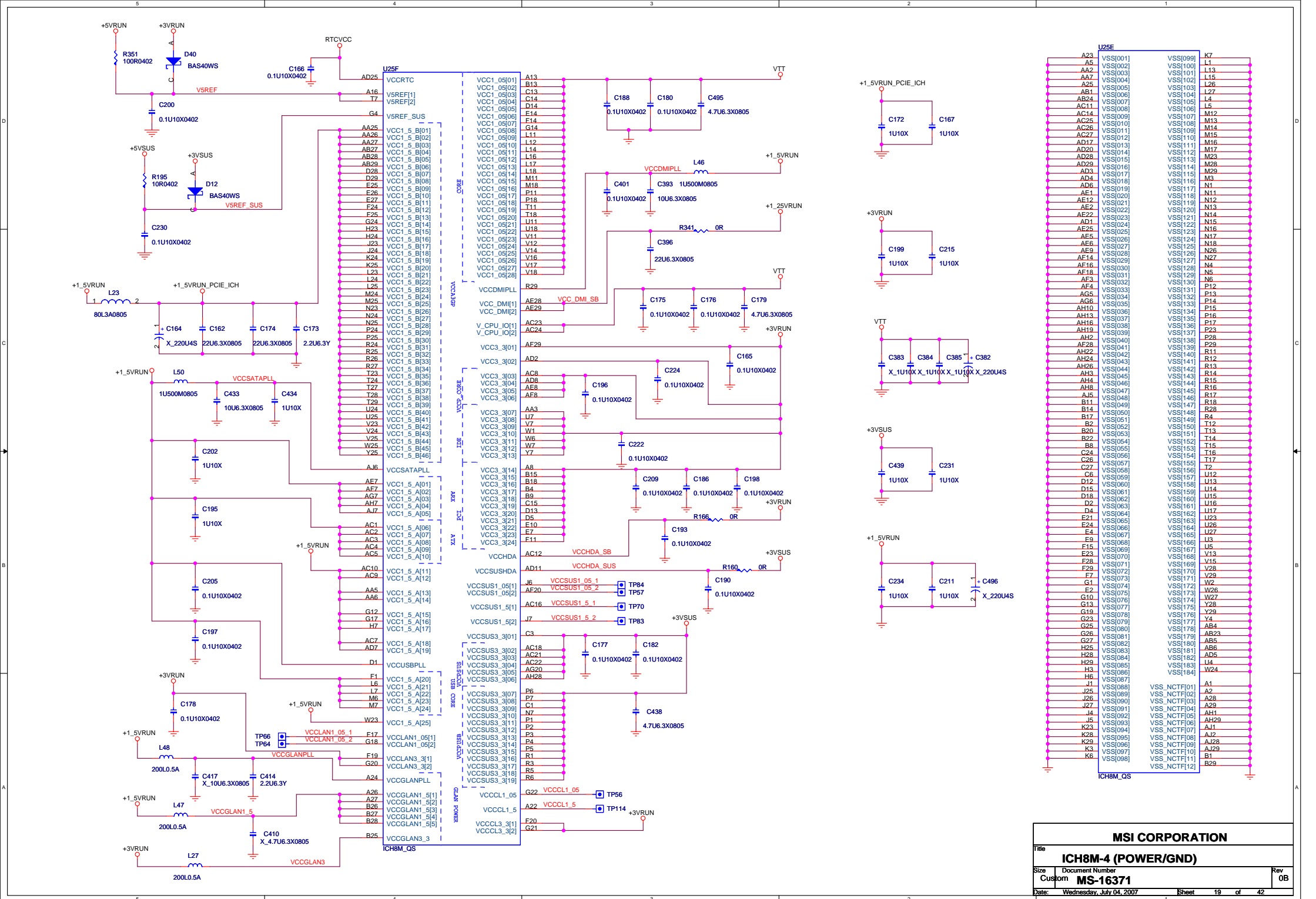
HDA_SDOUT (Default=Low)	HDA_SYNC (Default=Low)	GNT2# (Default=High)	GPIO20 (Default=Low)	GNT1#/GPIO51 (Default=High)	GNT3# (Default=High)	GNT0#/SPI_CS1# (Default=High)
XOR chain testing==>Low Set bit 1 of RPC.PC==>High	Set bit 0 of RPC.PC	Set bit 2 of RPC.PC2	Reserved	ESI Strap (server only)	Top-block swap mode ==>Low	Boot BIOS destination selection

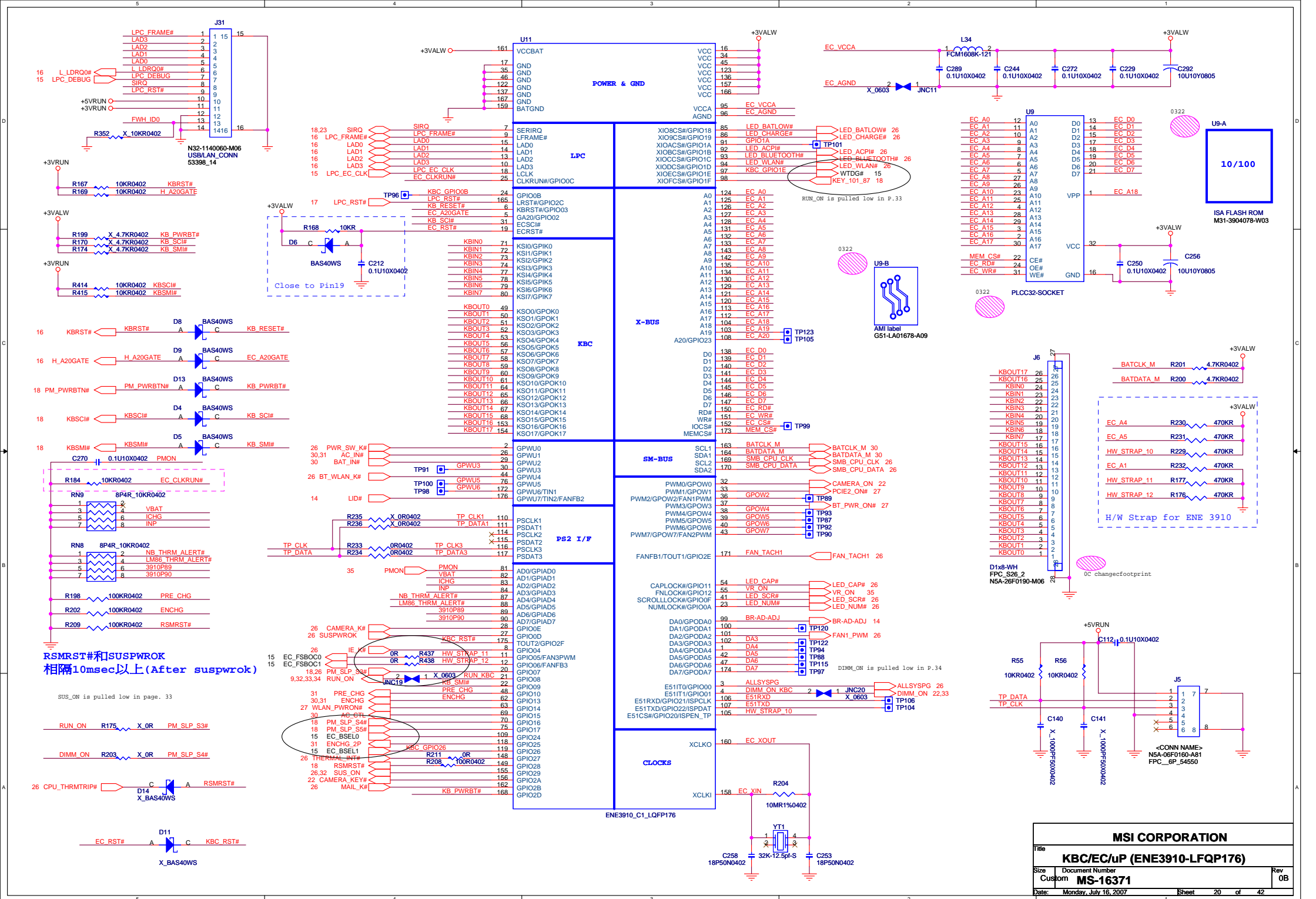
INTVRMEN	LAN100_SLP	SATALED# (Default=High)	SPKR (Default=Low)	TP3 (Default=High)	GPIO33/HDA_DOCK_EN# (Default=High)
Enable integrated Vccsusl_05, Vccsusl_5,VccCL1_5==High	Enable integrated VccLAN11_05,VccCL1_05==High	Set bit 27 of MPC.LR	No Reboot mode==>High	XOR chain Entrance	Flash Descriptor Security overridden==>Low Flash Descriptor will be in effect==>High

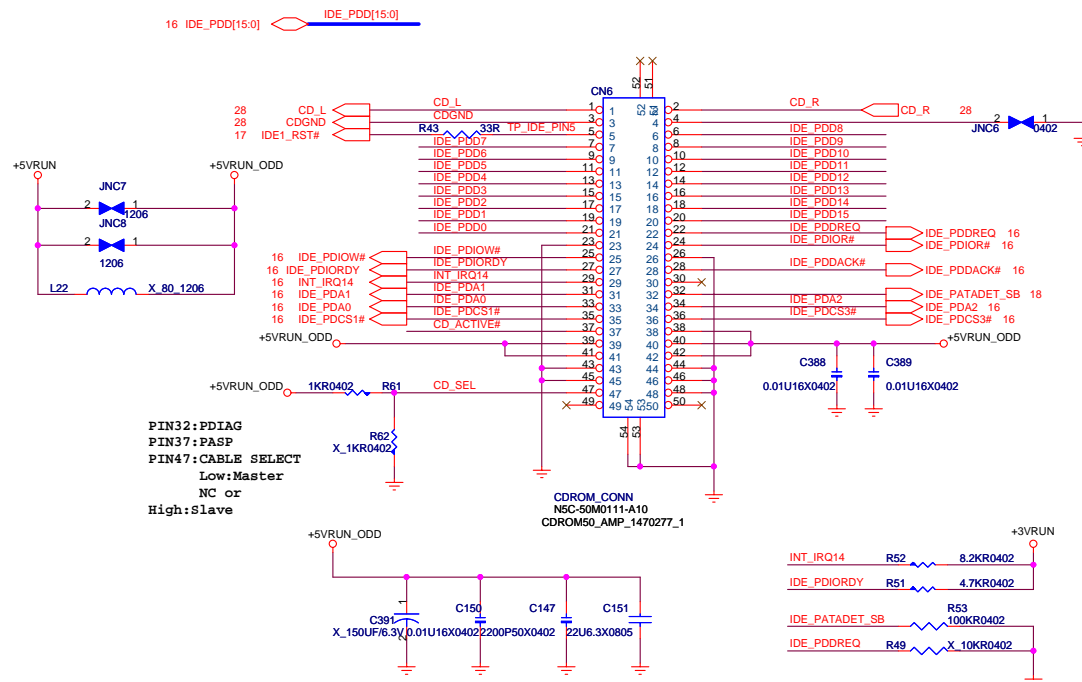
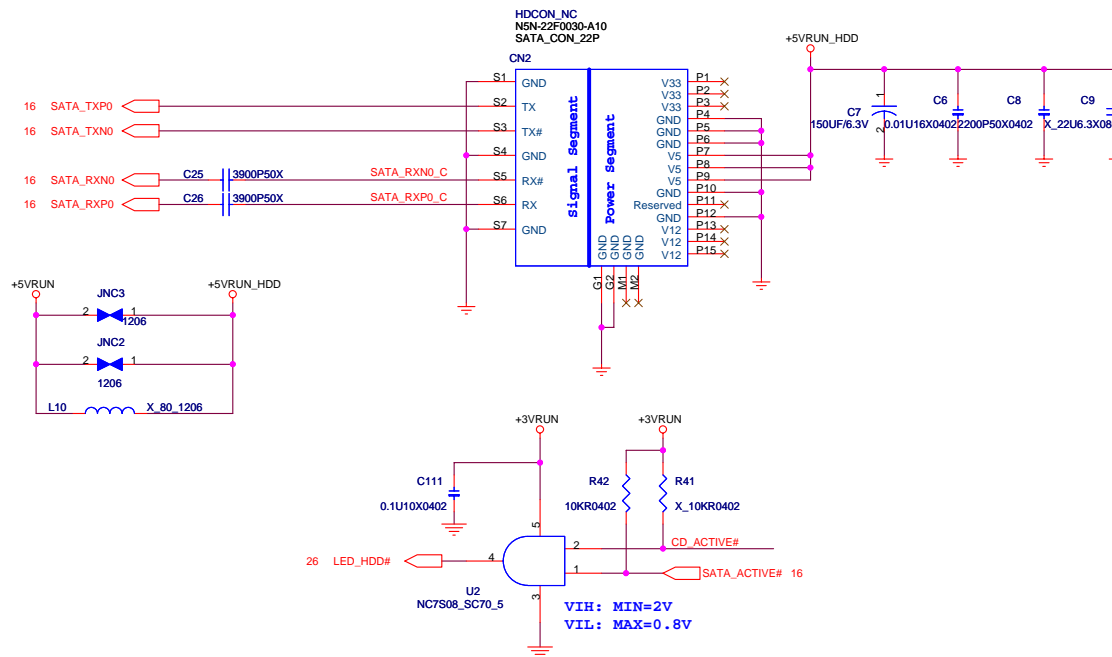
#### MSI CORPORATION

Title		
ICH8M-2 (PCI/USB/PCIE/DMI)		
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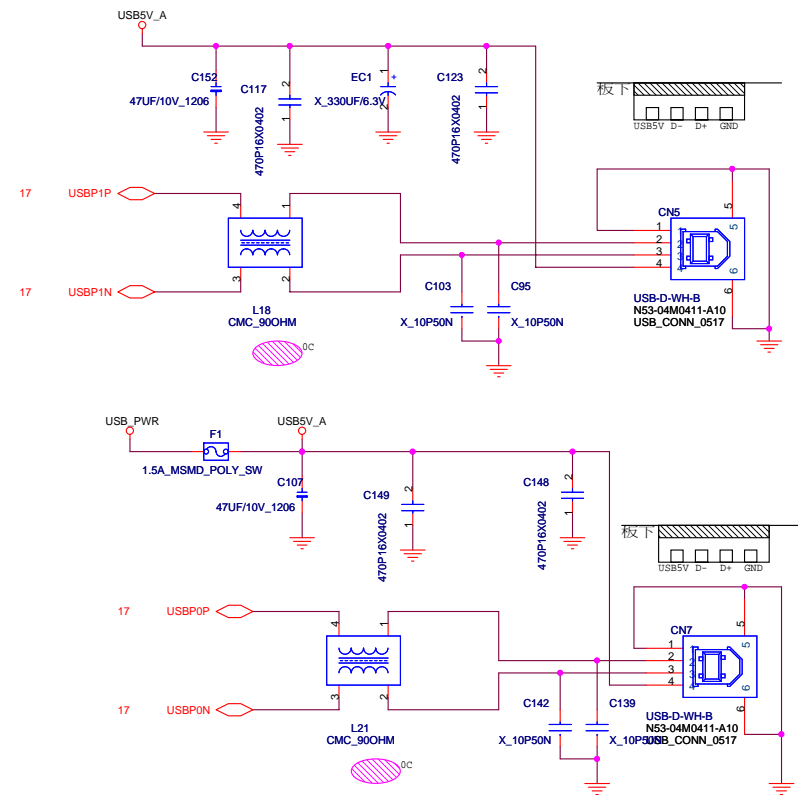
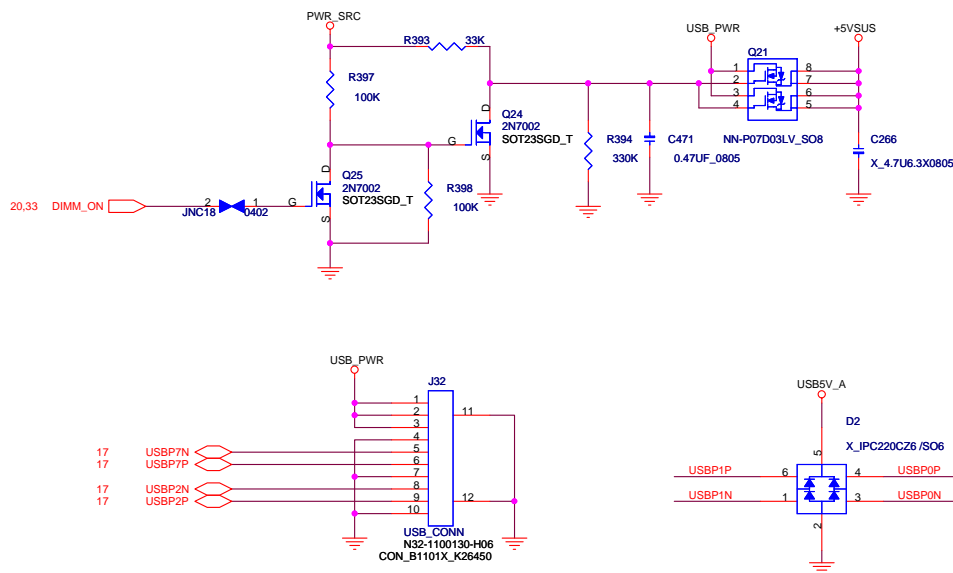




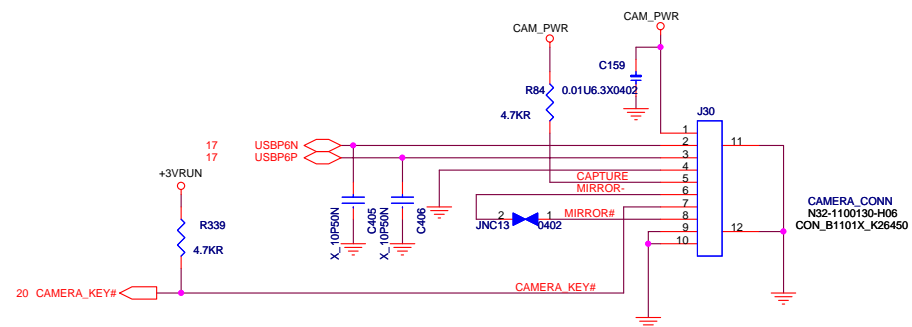
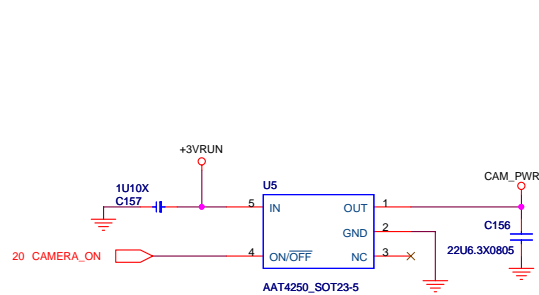




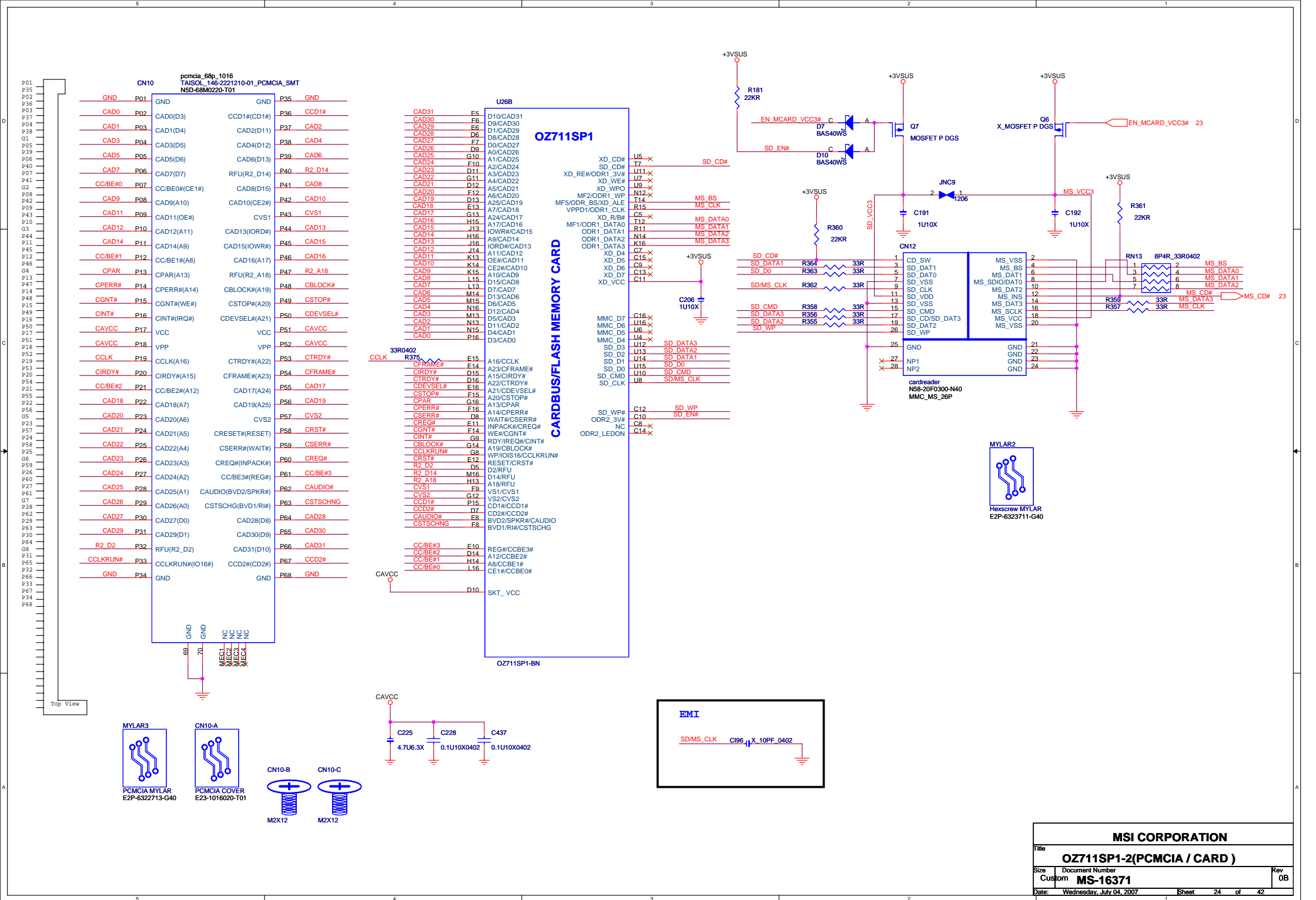
MSI CORPORATION			
Title	HDD&ODD		
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## DIGITAL CAMERA



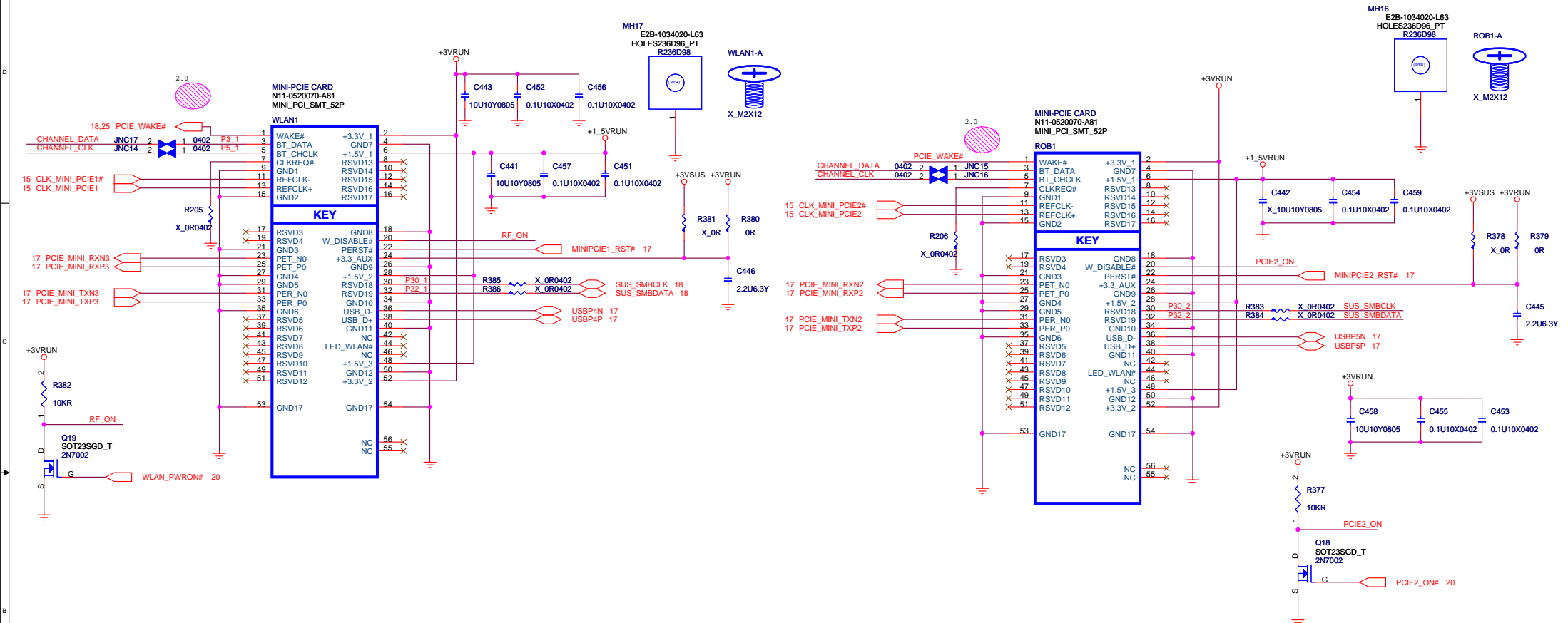




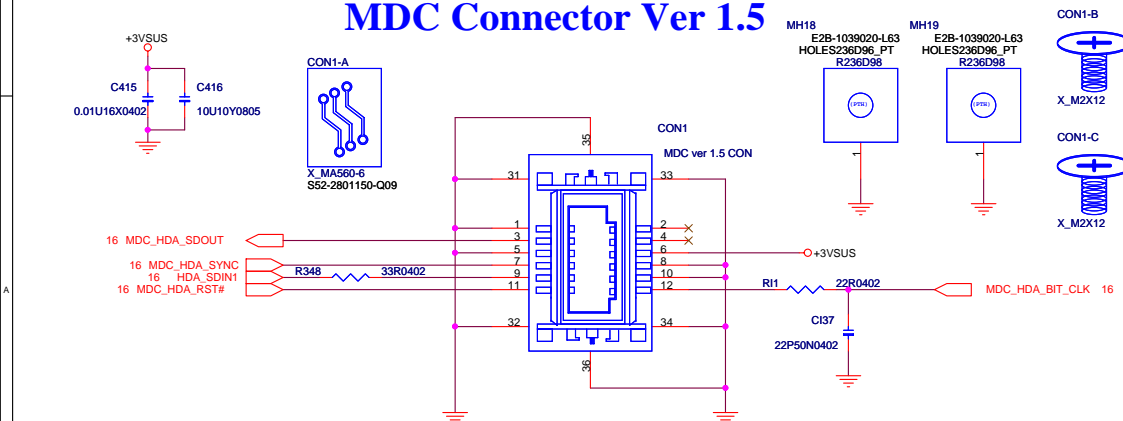




# WLAN and Robson(LG no need ROB1)

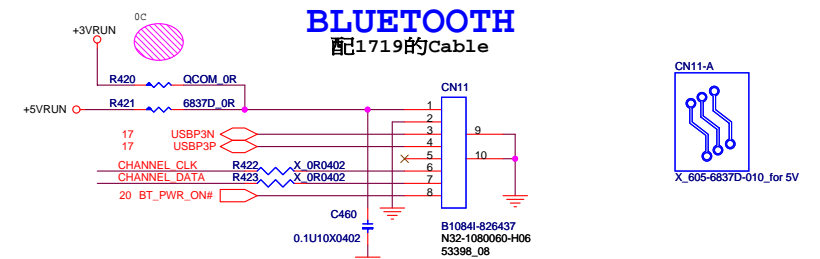


## MDC Connector Ver 1.5



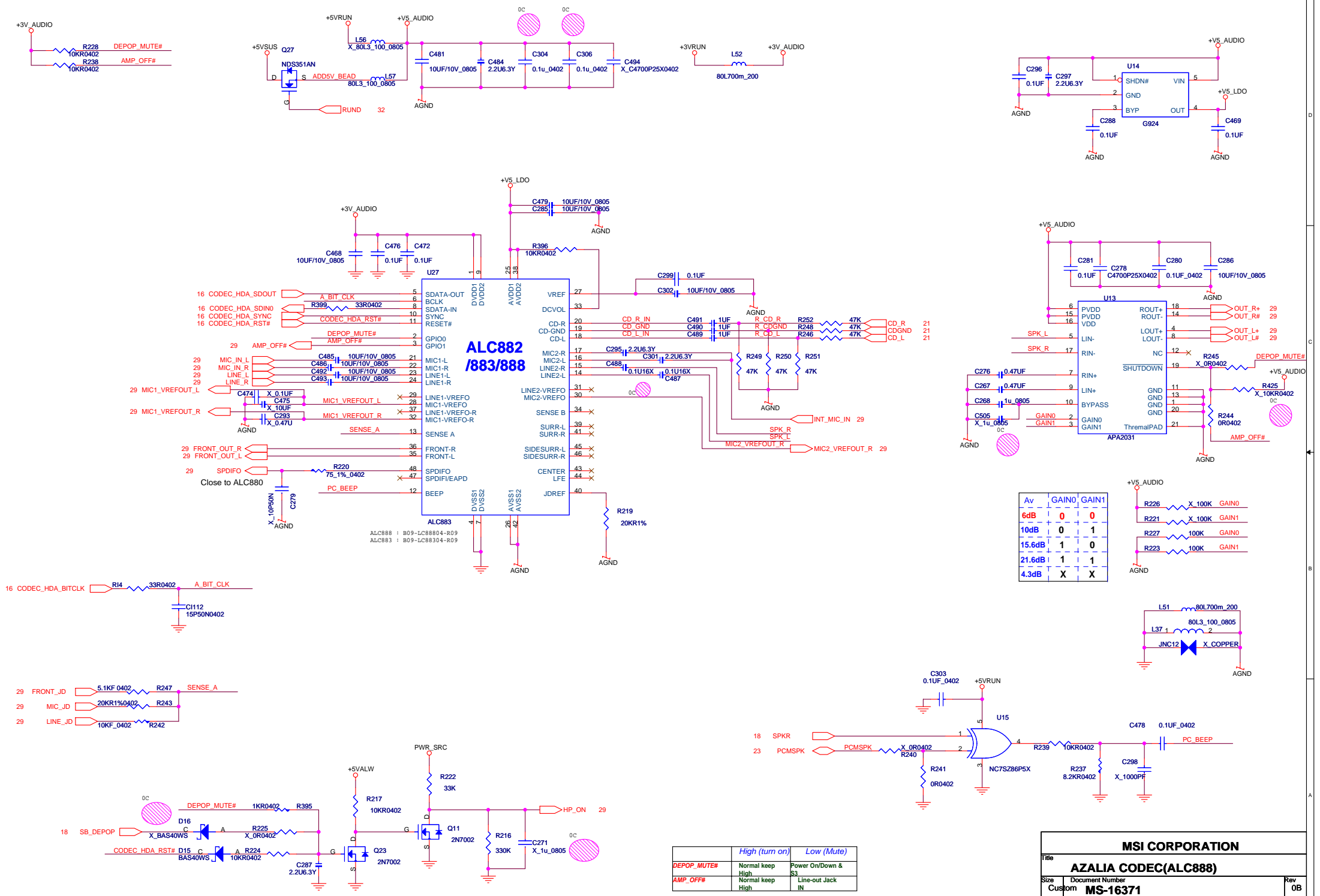
## BLUETOOTH

配1719的Cable



MSI CORPORATION

Mini PCIE & MDC & BT			Rev 0B
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Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X

	High (turn on)	Low (Mute)
DEPOP_MUTE#	Normal keep High	Power On/Down & S3
AMP_OFF#	Normal keep High	Line-out Jack IN

MSI CORPORATION

Title

AZALIA CODEC(ALC888)

Size

Document Number

Rev

OB

Date

Wednesday, July 04, 2007

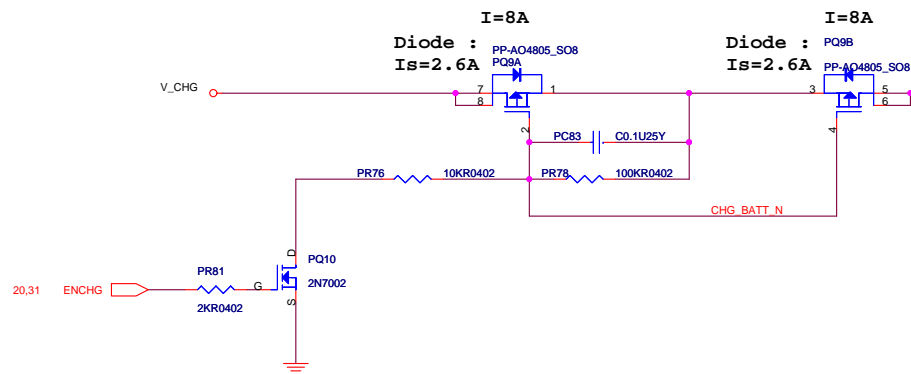
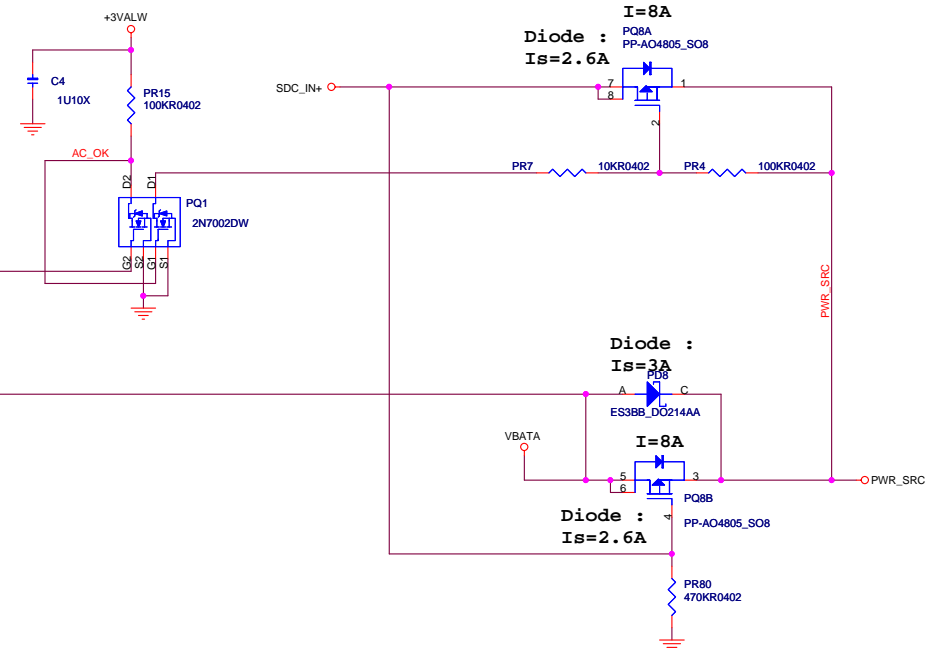
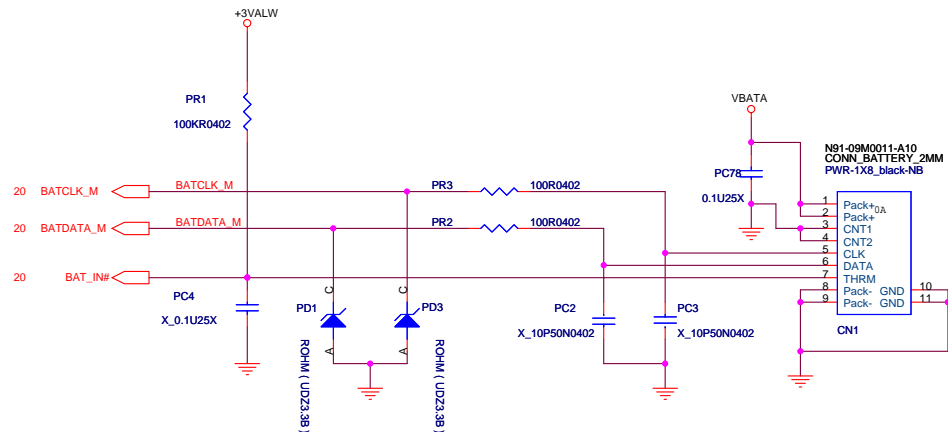
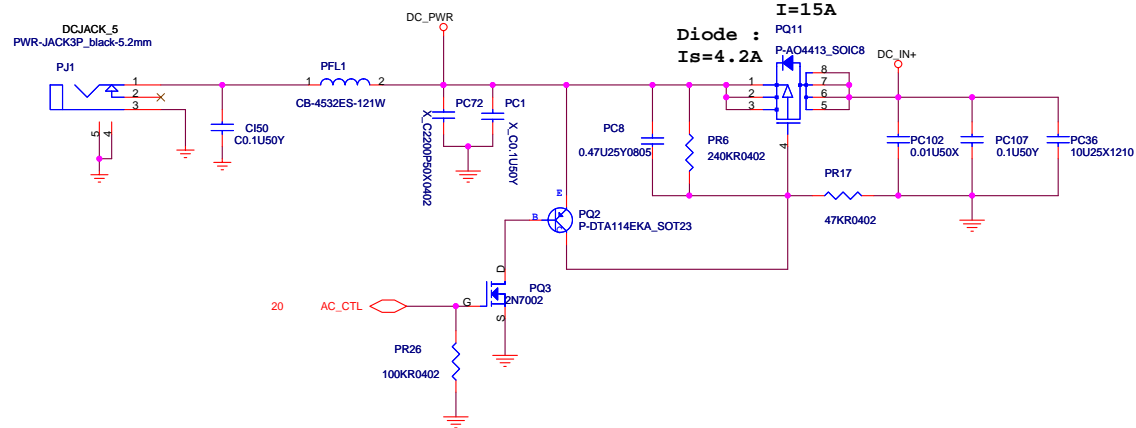
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MSI CORPORATION			
Title			
Battery Select			
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Adapter= 90 W  
 Adapter input voltage set 17.4 Voltage  
 If <17.4V, ACOK#=high

CELL GND=2 CELLS  
 FLOAT=3 CELLS  
 REFIN=4 CELLS

3S2P: Charge current set 3 Amp  
 3S3P: Charge current set 4.5 Amp  
 Pre-charger: Charge current set 220mA

20 PRE\_CHG  
 20 ENCHG\_2P  
 20,30 AC\_IN#

+5VALW  
 20,30 ENCHG

65W\_DETEC : DEFAULT=HIGH  
 High =>65W  
 Low =>90W

90W for LG

need to check value

SET Iin MAX = A

Input=(Vcls/Vref)\*(0.075/RS1)  
 RS1=PR74=0.01, Vref=4.096V  
 Vcls=4.096\*PR23/(PR23+PR97)=2.29V  
 Input=(2.29/4.096)\*(0.075/0.01)=4.2A

PR23	PR97	
19.1K	28.7K	65W
	24K	75W
	16.9K	90W

ENCHG-2P	PRE_CHG	ENCHG	
0	1	1	Pre-charge
1	0	1	3S2P-Fast charge
0	0	1	3S3P-Fast charge
0	0	0	STOP CHARGE

Icharge=(Vicl1/Vrefin)\*(0.075/RS2)  
 RS2=PR24=0.015  
 Vrefin=MAX8724\_LDO\*PR35/(PR34+PR35)  
 =5.4V\*1.1K/(1.1K+768)=3.18V=MAX8724\_REFIN  
 Vicl1=MAX8724\_REFIN\*PR30/(PR11+PR30)

For 3S2P:  
 Vicl1=3.18\*(PR30/(PR108))/((PR30/(PR108))+PR11)  
 =3.18\*15.91K/(15.91K+10.5K)=1.92V  
 Icharge=(1.92/3.18)\*(0.075/0.015)=3.01A

For 3S2P:  
 Vicl1=3.18\*PR30/(PR30+PR11)  
 =3.18\*95.3K/(95.3K+10.5K)=2.86V  
 Icharge=(2.86/3.18)\*(0.075/0.015)=4.5A

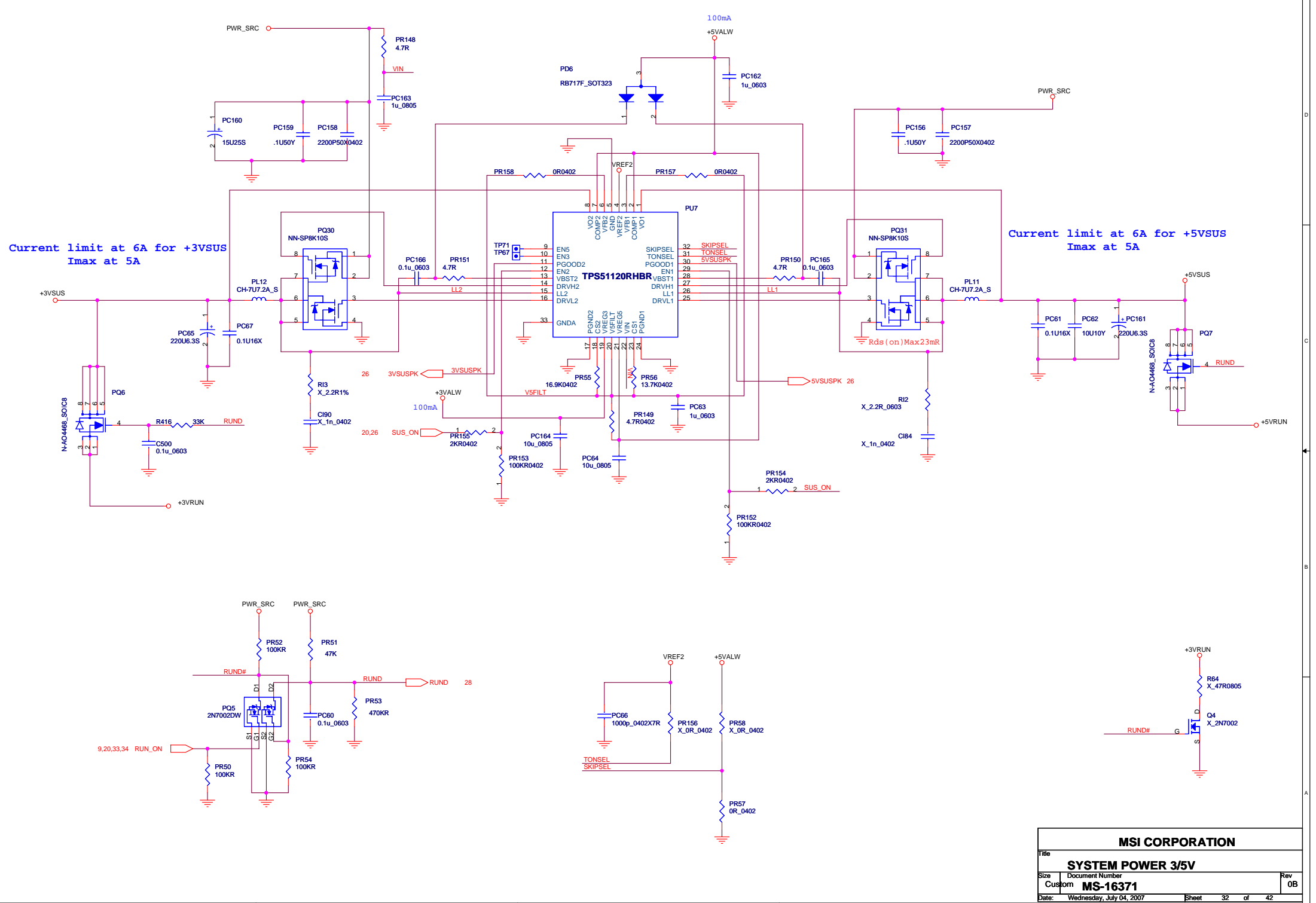
For Precharge:  
 Vicl1=3.18\*(PR30/(PR105))/((PR30/(PR105))+PR11)  
 =3.18\*0.496/(0.496+10.5K)=0.15mV  
 Icharge=(0.15mV/3.18)\*(0.075/0.015)=0.236mA

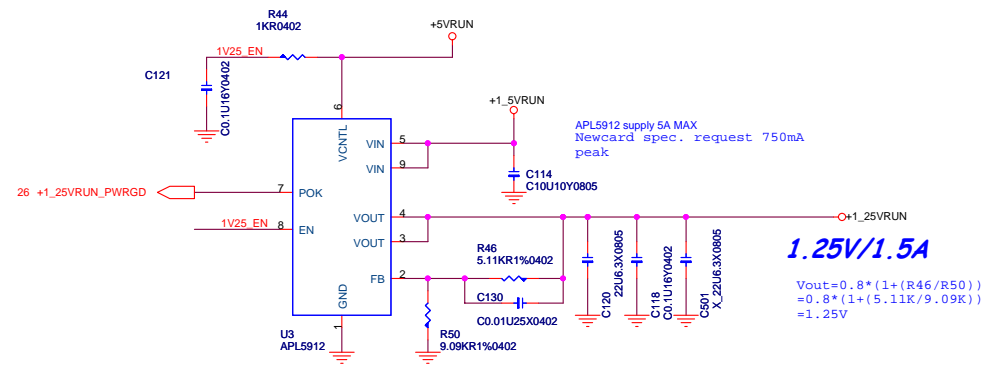
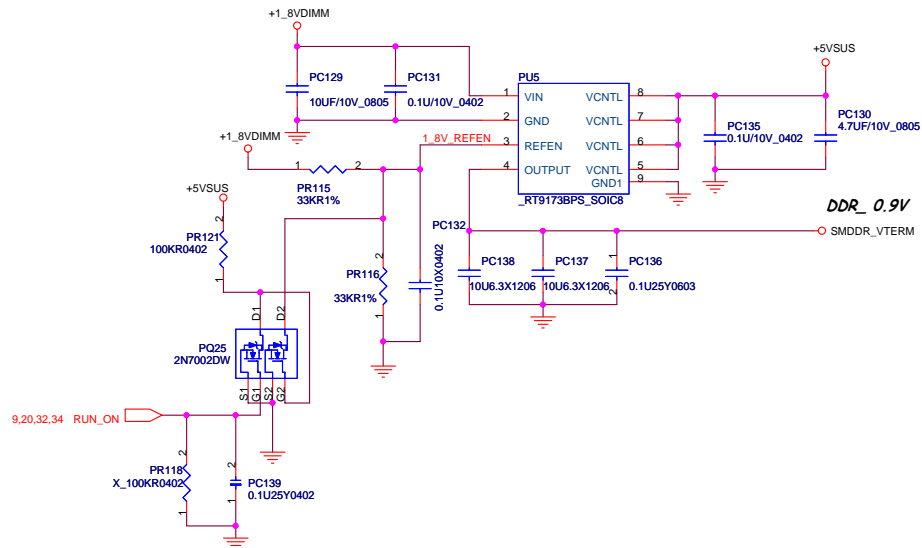
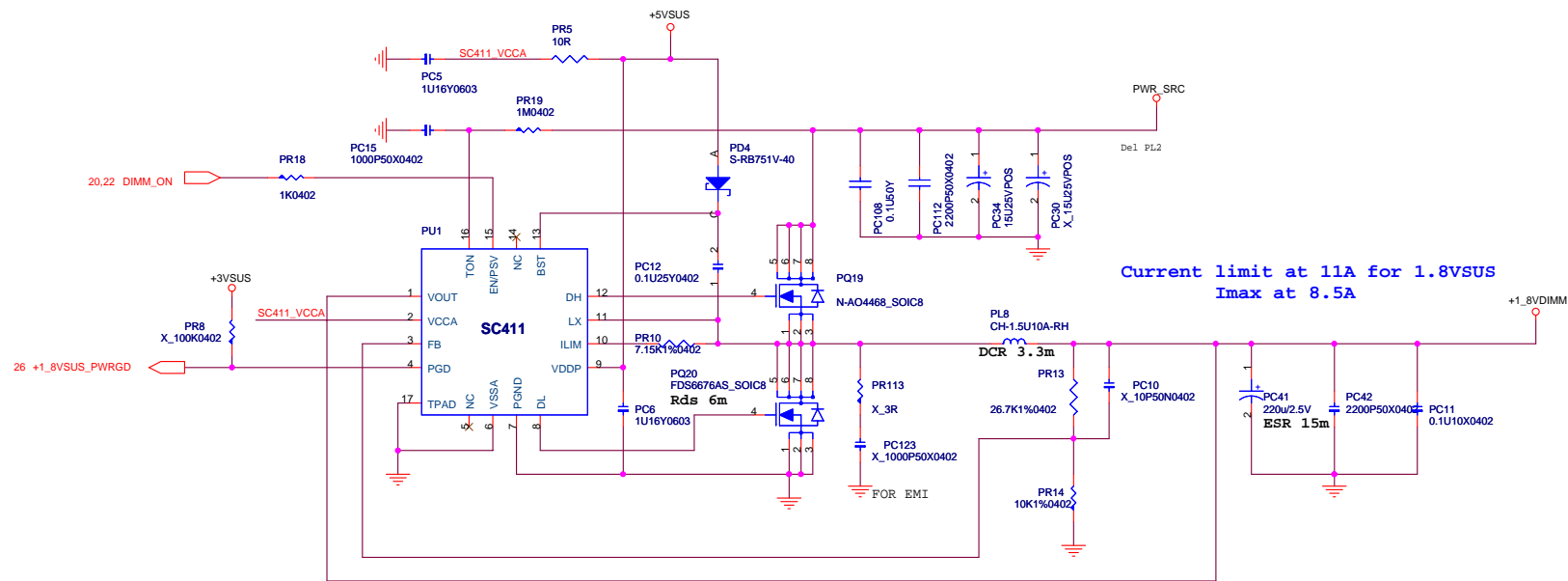
MSI CORPORATION

Title			
Battery Charger			
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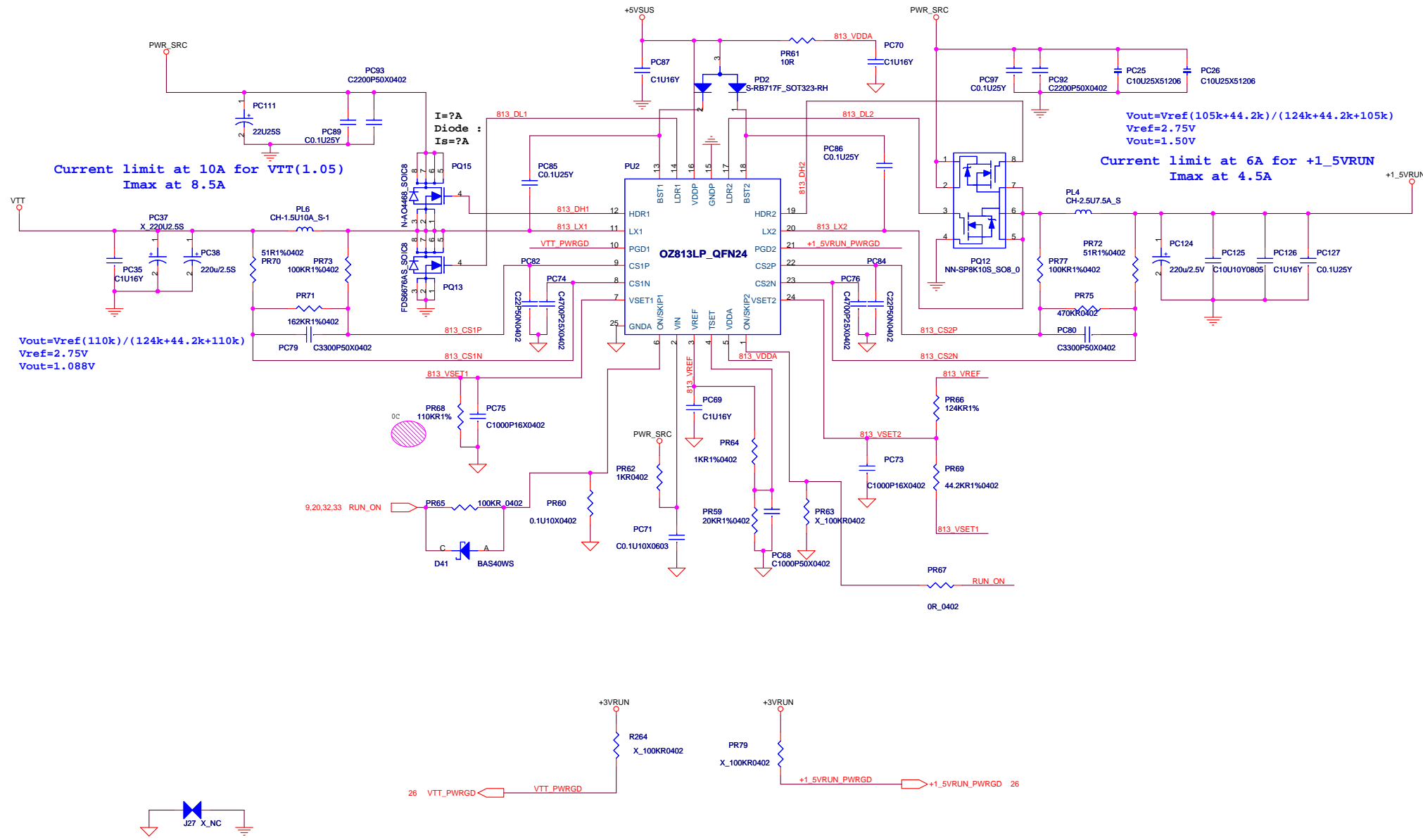
Current limit at 6A for +3VSUS  
Imax at 5A

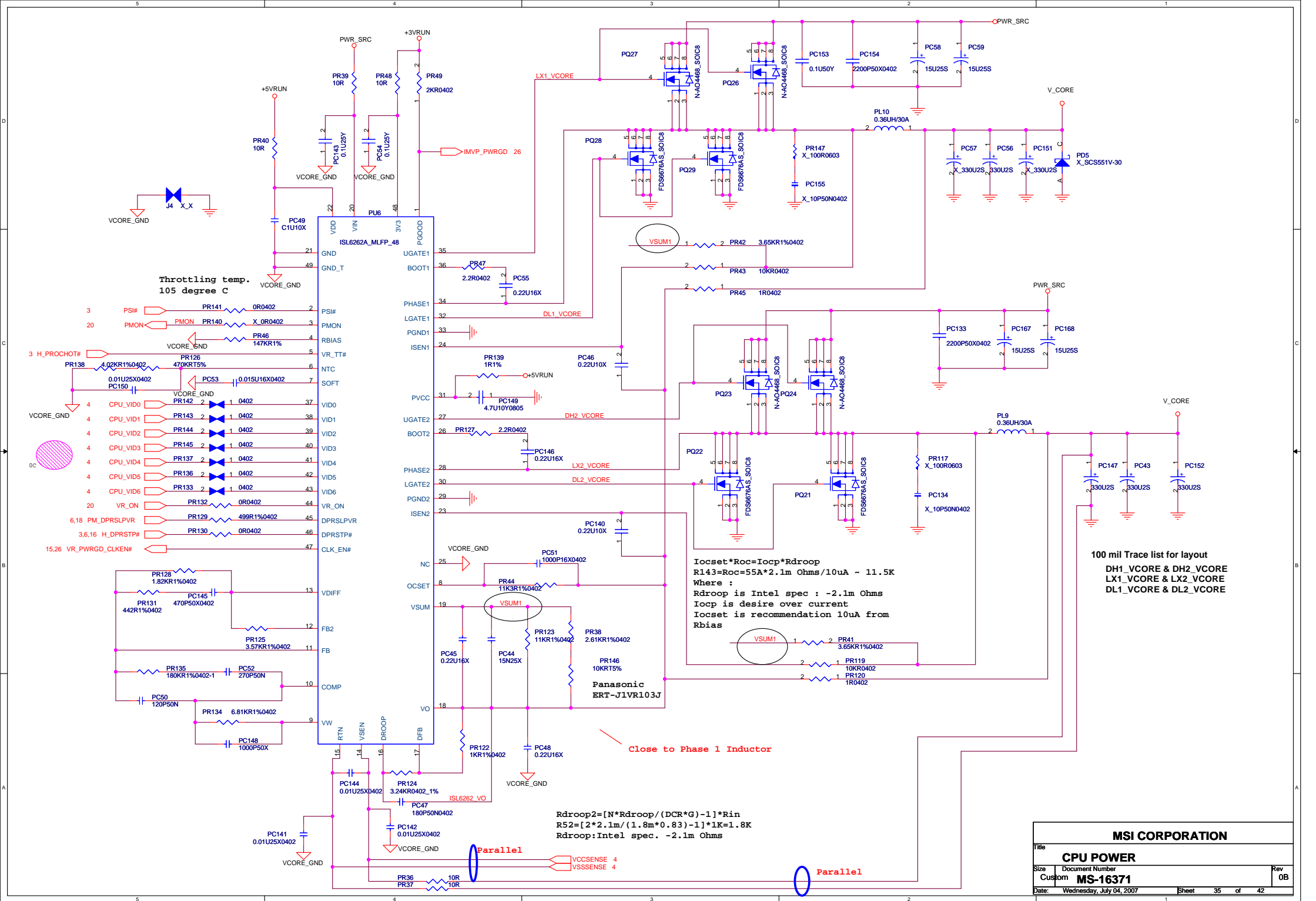
Current limit at 6A for +5VSUS  
Imax at 5A





MSI CORPORATION			
File			
DDR2 RAM POWER, +1.25V			
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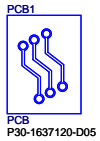
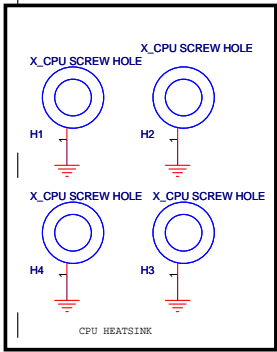
FDE single high  
should be < 3.3V

Current limit at 15A for +VGFX\_CORE(0.7~1.25V)  
Imax at 8A

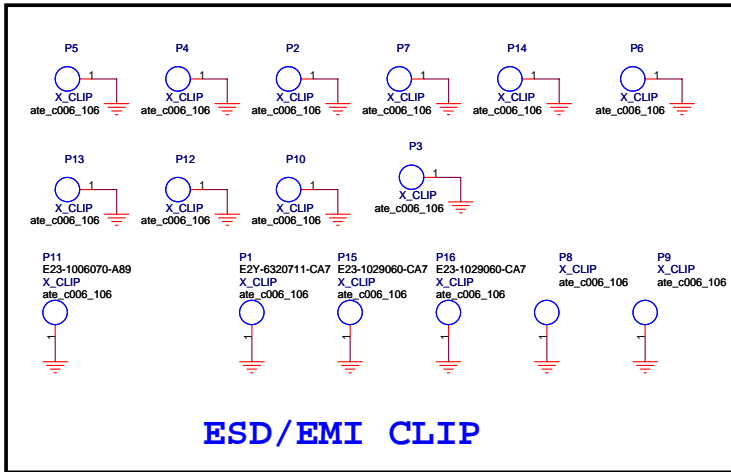
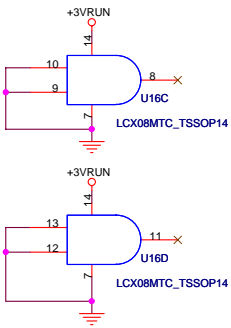
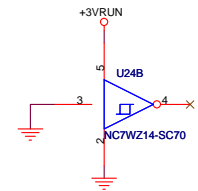
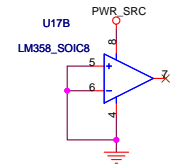
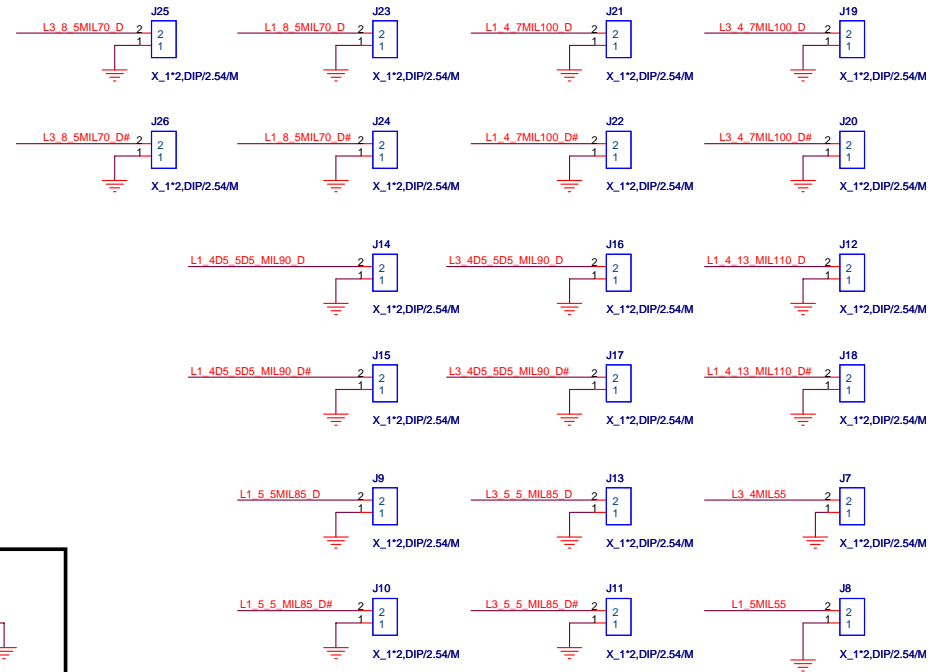
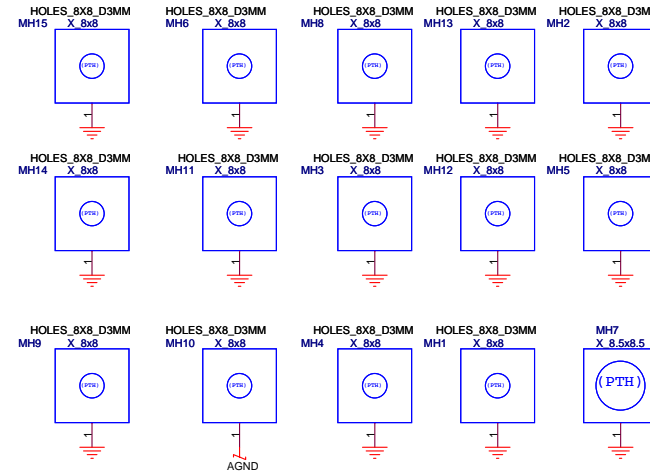
$I_{ocset} * R_{oc} = I_{ocp} * R_{droop}$   
 $R_{191} = R_{oc} = 15A * 8m\ Ohms / 10uA \sim 12.1K$   
 Where :  
 $R_{droop}$  is Intel spec : -8m Ohms  
 $I_{ocp}$  is desire over current  
 $I_{ocset}$  is recommendation 10uA  
 from Rbias

Intel workaround :  
fixing "system may not boot".  
 $GFX\_VID\_ [3:0] = 0011 \rightarrow 1.13V$

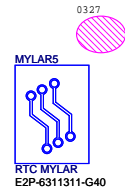
$R_{278} \ 22KR0402$   $X_{22KR0402}$   $R_{279} \ 22KR0402$   
 $GFX\_VID\_0\_R$   
 $R_{277} \ 22KR0402$   $X_{22KR0402}$   $R_{276} \ 22KR0402$   
 $GFX\_VID\_1\_R$   
 $R_{271} \ X_{22KR0402}$   $R_{272} \ 22KR0402$   
 $GFX\_VID\_2\_R$   
 $R_{269} \ X_{22KR0402}$   $R_{270} \ 22KR0402$   
 $GFX\_VID\_3\_R$



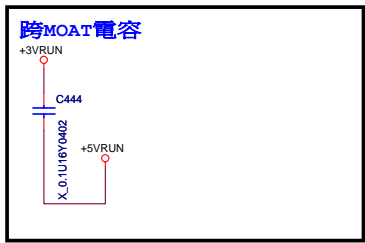
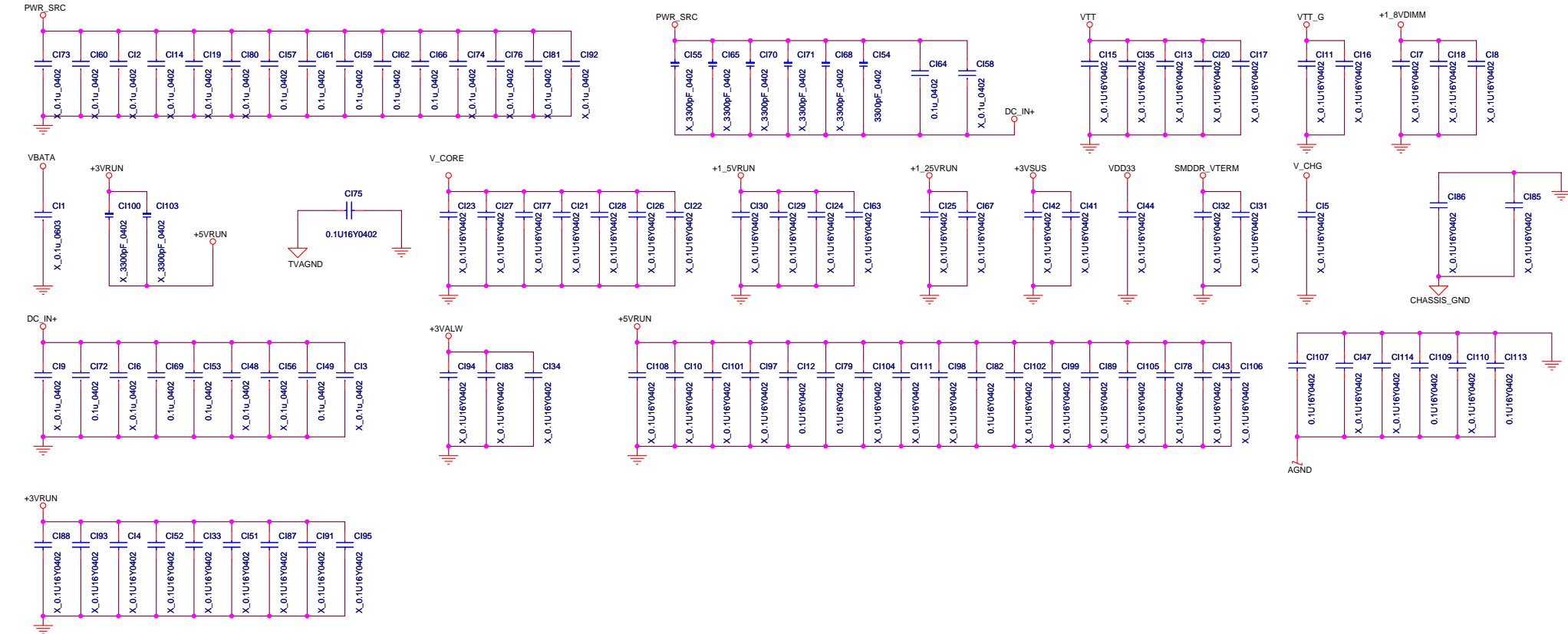
P30-1637120-H73,瀚宇博德  
P30-1637120-Y34,元茂  
P30-1637120-D05,昆穎(定穎大陸)



ESD/EMI CLIP

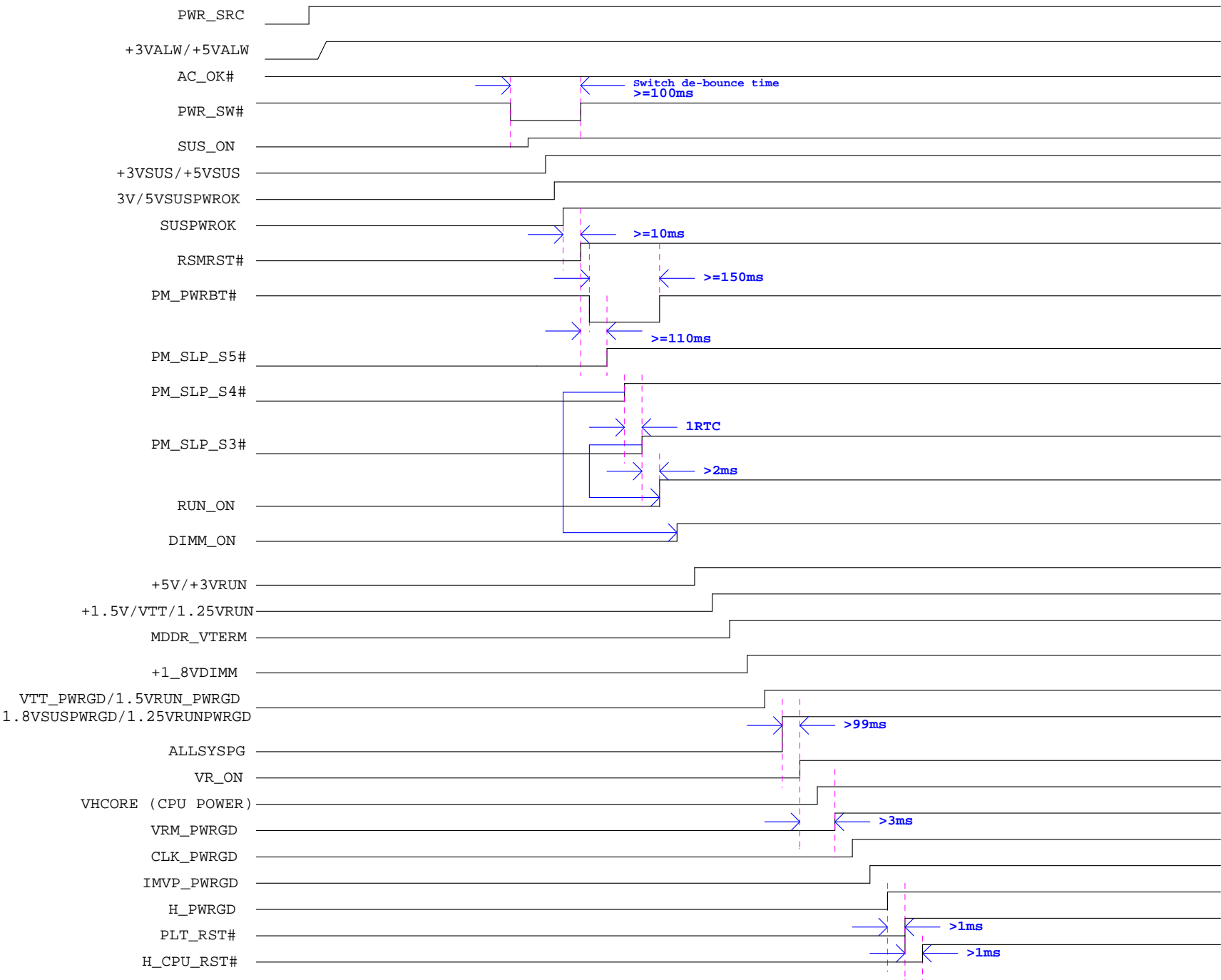


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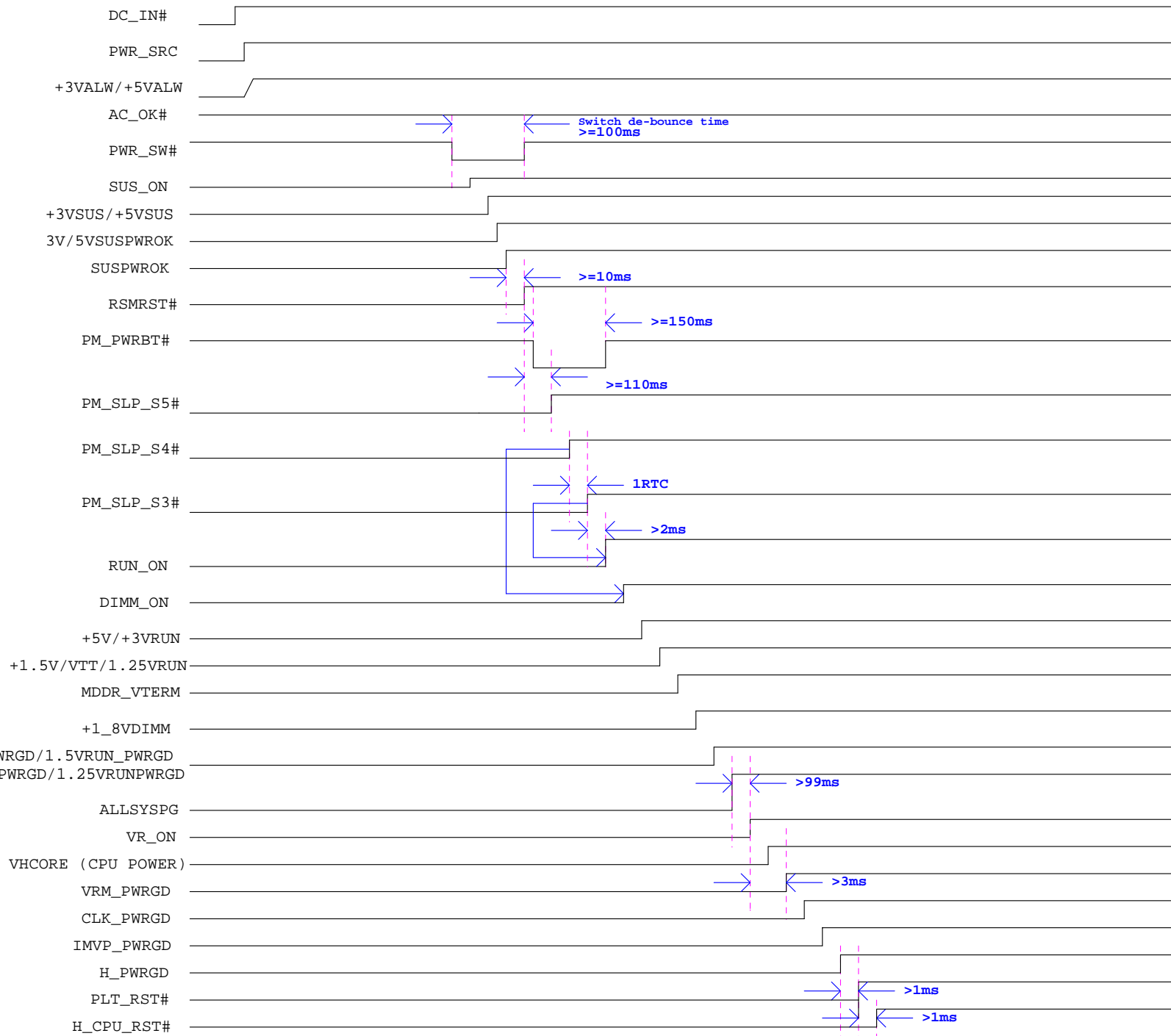


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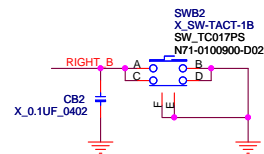
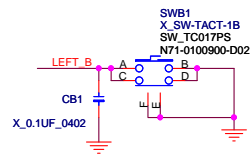
SANTA ROSA System Power on Sequence Battery MODE (S5->S0)



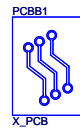
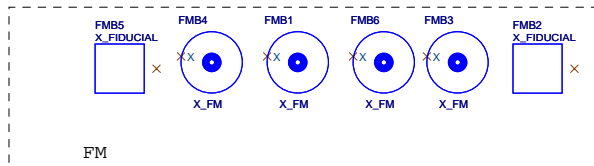
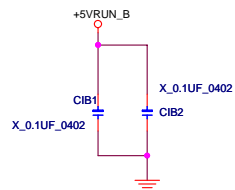
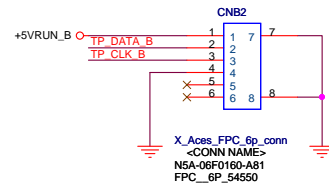
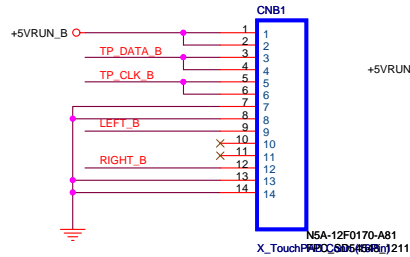
# SANTA ROSA System Power on Sequence (G3->S0)



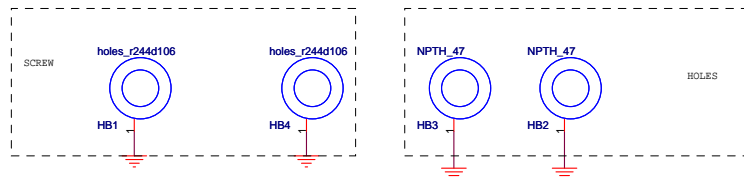
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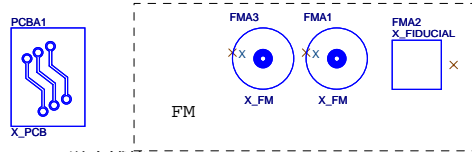
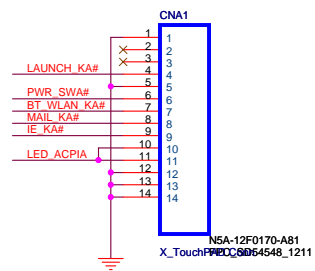
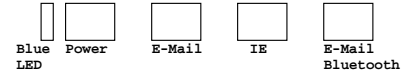
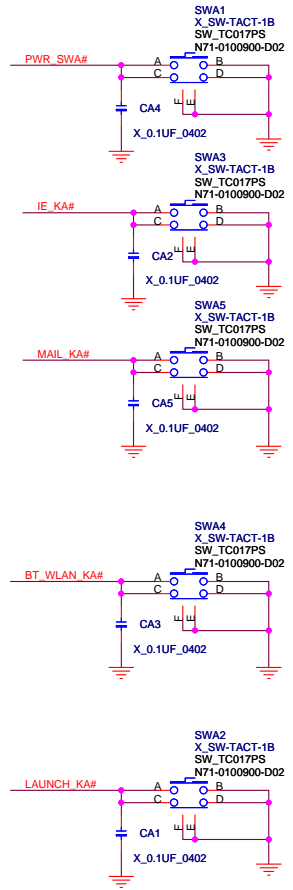
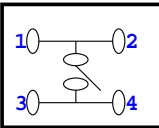
For TM61P-307 pin define



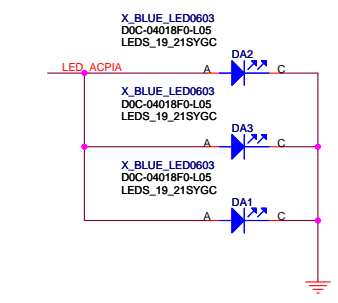
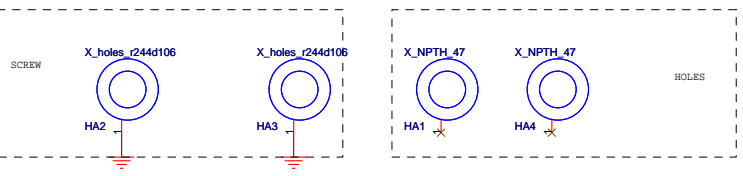
P30-1637B10-H73,瀚宇博德  
P30-1637B10-Y34,元茂  
P30-1637B10-D05,昆穎(定穎大陸)



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P30-1637A10-D05,昆穎(定穎大陸)



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